GaN-on-Si Reliability:
A Comparative Study between Process Platforms.

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Abstract

GaN-on-Si transistors are put through an extensive suite of reliability tests in order to accurately assess the drift characteristics of the technology. Data is presented on DC-HTOL, RF-HTOL, and 3-temperature DC tests. In all cases results are compared with the previous generation of technology and reveal improved results. Highlights include an increase in the activation energy from 1.7eV to 2.0eV and a 50% reduction in the 20-year drift rate as predicted by DC-HTOL testing.

I. Introduction

GaN-based transistors have long been targeted for insertion in a number of high power RF applications. Recently GaN devices are realizing this potential and seeing insertion in real work applications. Nitronex has released its NRF1 process platform, the first process for comercial use, and to date has qualified five RF products based on this process. In this paper we compare results shown at last year's ROCS conference on the PH7 process platform with those obtained on the recently released NRF1 platform [1]. Results are shown for many of these electrical tests including 3-temperature DC, DC-HTOL, and RF-HTOL.

II. Background

The NRF1 process platform was released for product development in October of 2005 and to date over 200 wafers have been processed. NRF1 incorporates several key process changes when compared to the previous PH7 baseline. There were several motivations for the changes. For instance, the gate length was reduced to improve gain and support operations at 3.5GHz, a source field plate was included to improve high voltage performance, and the gate anneal was implemented to improve reliability. A summary of the process differences between PH7 and NRF1 is listed in Table 1 below.

Table 1: Comparison of PH7 and NRF1 process features.

	PH7	NRF1
Epitaxial Commodity	01038-4	04001-0
Gate Length	0.7μm	0.5μm
Configuration	standard	source-plate
Gate Anneal	No	Yes
Encapsulation Process	SiNx 90/400nm	SiNx 90/400nm
Die Thickness	6mil	6mil

Aside from these modifications other aspects of the process are carried over from the previously qualified PH7 process. These similarities include the general epitaxial design, the gate and ohmic contacts, plated airbridges, SiNx passivation, and backside thinning and via processing.

NRF1 is Nitronex's first process platform that will be used to support commercial products. The first of these products is the NPT35050 device and as such this device served as the qualification vehicle to be used in all reliability tests described below. The NPT35050 consists of a 36mm transistor die attached into a high thermal conductivity CPC single-ended, ceramic package using a AuSi eutectic attach process. The sources were grounded to the package base through backside vias in the 150μm-thick silicon die. A 2-stage internal matching network is used to transform the input impedance, while no intentional internal matching exists on the output. The typical CW performance of these devices includes 60-70W saturated output power at an operating voltage of 28V and frequency of 3.5GHz [2]. A photograph of the NPT35050 device can be seen in Fig. 1.

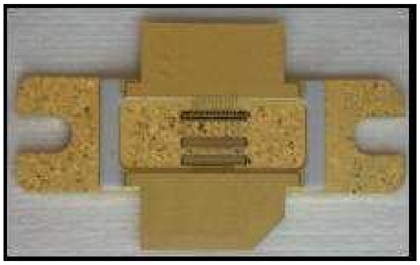

Figure 1: Photograph on NPT35050 device consisting of 36mm die with 2-stage input match in CPC ceramic package.

The qualification for the NRF1 platform included repeating all tests performed on PH7 with larger sample sizes as well as the addition of 10 new tests to more thoroughly characterize the reliability. A comparison of all reliability tests performed on PH7 and NRF1 is shown in Table 2. This paper focuses on the fundamental tests which are common to the PH7 and NRF1 data set and provides comparisons between drift characteristics for the two technologies.

Table 2: Comparison of qualification tests performed on PH7 and NRF1 process platforms.

Test Name	Test Standard	PH7 Sample Set	NRF1 Sample Set
DC-HTOL	JESD22-A108	30 Devices, 1000 hours	45 devices, 1000 hours
3-Temp DC	JEP118-B	10 Devices/Temp @ 260, 285, and 310°C	30 Devices/Temp @ 260, 285, and 310°C
RF-HTOL	JESD22-A101-A	8 Devices, 500 hours	6 Devices, 500 hours
ESD-HBM	M-750-1020	30	36
ESD-MM	M-750-1020	30	36
Thermal Impedance	–	10	36
Autoclave	JESD22-A102	10	45
VSWR	–	10	36
Temp. Cycling	JESD22-A104	--	45
Thermal Shock	M-750-1056	--	15
Solderability	JESD22-B102	--	4
Mech. Shock	M-883-2002	--	38
Vibration	M-883-2007	--	38
Const. Acceleration	M-883-2001	--	38
Moisture Res.	M-883-1004	--	38
Salt Atmosphere	M-883-1009	--	15
Solvent Res.	M-833-2015	--	15
Bond Strength	M-750-2037	--	15

III. RESULTS & DISCUSSION

When characterizing the reliability performance of a technology it is important to look at the drift characteristics under a variety of test conditions. The NRF1 technology was characterized through the use of 3-temperature DC testing, DC-HTOL testing, and RF-HTOL testing. For all test methods the NRF1 technology is compared with the previous PH7 performance.

A. 3-Temperature DC

3-Temperature DC testing was carried out at temperatures of 260°C, 285°C, and 310°C. In all cases devices were biased at V_{DS}=28V and I_{DS}=2.34A with the ambient temperature varied to achieve the desired junction temperature. IR thermal imaging was performed prior to lifetest to confirm the temperature settings. Sample size consisted of 25-30 devices from 3 process lot in each temperature group. The stress time was 250 hours for the highest temperature and 1000 hours for the lowest temperature. The in-situ drain current is monitored on each device and a 15% drift is used as a failure criteria.

Plotting the data on a cumulative failure plot reveals an excellent fit to a lognormal distribution, as seen in Fig. 2. This plot shows the time to fail for each device with 90% confidence limits. In Fig. 3, the MTTF for each temperature is plotted on an Arrhenius plot and reveals an activation energy of 2.0eV for the NRF1 process platform. For comparison the 3-temperature data is also plotted for the PH7 technology, which utilized a similar device geometry and test conditions (temperatures, bias, etc). The comparison reveals a slightly higher activation energy for the new NRF1 process and a similar MTTF of $>10^7$ hours at an operating temperature of 150°C.

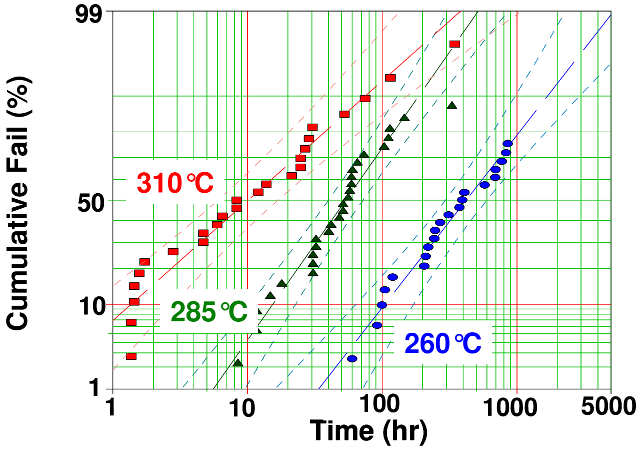

Figure 2: Cumulative failure plot showing lognormal distribution.

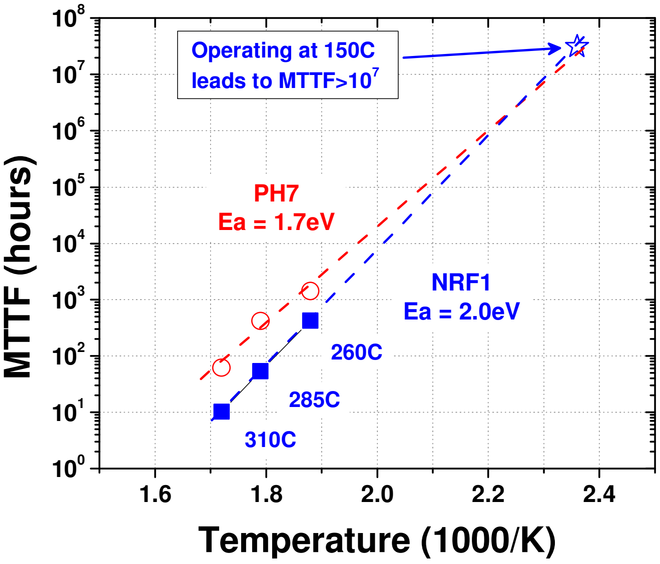

Figure 3: Arrhenius plot showing activation energy for PH7 (open) and NRF1 (solid) process platforms.

B. DC-HTOL

DC-HTOL is currently being performed on 45 devices from 3 process lots. The stress temperature is 200°C with bias set at V_{DS}=28V and I_{DS}=2.34A. Devices are to be stressed for

1000 hours with a full suite of DC and RF characterization prior to lifetest and at intermediate test intervals of 36 hours, 168 hours, 500 hours, and 1000 hours. At the time of publication test has completed 300 hours of stress and those results are shown here.

The box plots in Fig. 4 show the pinch-off voltage at each test interval. In Fig. 5 the means of maximum drain current for each test interval are plotted on a log-based time scale. For comparison the PH7 results are also plotted in the same graph. The data reveals a 50% improvement in drift for the NRF1 process. This confirms initial results shown last year following a failure analysis study an implementation of process improvements in the form of a gate anneal [3, 4].

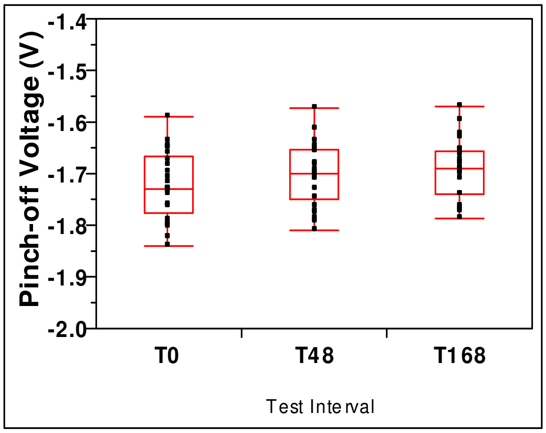

Figure 4: Box plots showing distributions for pinch-off voltage at each test interval.

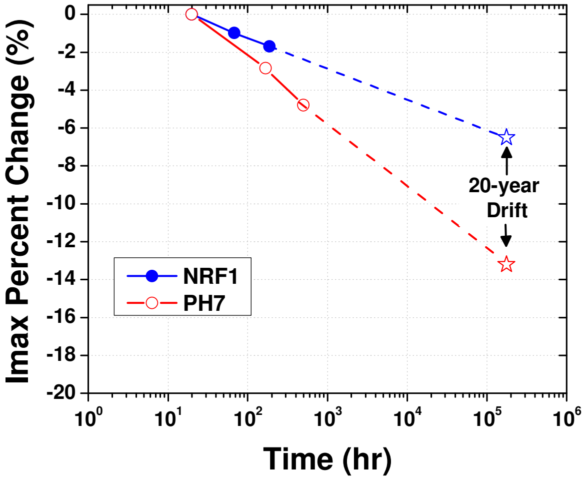

Figure 5: Comparison of drift in maximum current for PH7 (open) and NRF (solid) process platforms.

The previously established activation energy of 2.0eV is used to convert the 200°C HTOL data to a more practical operating condition of 150°C. Figure 6 shows 20-year drift rates less than 3% at junction temperature of 150°C and 6% at 200°C.

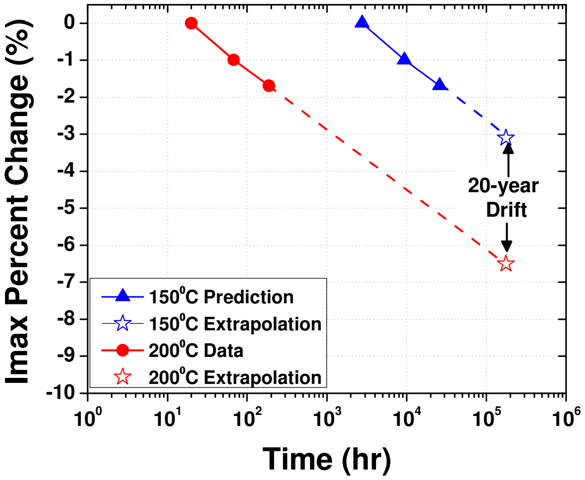

Figure 6: Imax drift as measured at 200°C and after applying deceleration factor at 150°C.

C. RF-HTOL

RF-HTOL testing was carried out in order to verify that the addition of RF stimulus did not induce any additional failure mechanisms. A total of 6 samples were stressed at V_{DS}=28V, Freq=2.14GHz, and Pin sufficient to drive the device into 3dB gain compression with the baseplate adjusted to produce a T_j=200°C. Figure 7 shows the drift in the in-situ P_{out} versus time for the 6 samples.

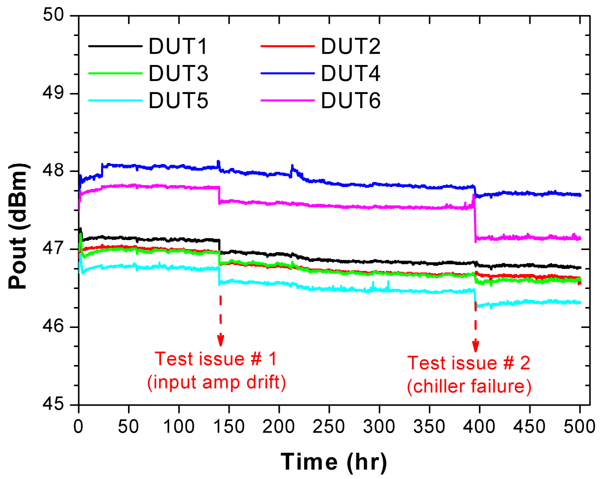

Figure 7: RF-HTOL results for 6 devices at V_{DS}=28V, P_{out}~47dBm, and T_j=200°C.

There were two test issues which lead to systematic shifts in the data. The first issue occurred around 130 hours and was a drift in the input amplifier causing the Pin delivered to the devices to drop ~0.25dB. The second issue occurred at 388 hours and involved a chiller failure which caused the junction temperature to rise significantly before the devices were powered down. Some devices experienced junction temperatures as high as 400°C for 10-20 minutes. After resetting the junction temperature all devices came back to within 0.2dB of original value except DUT 6 which lost about 0.5dB in performance.

In previous test runs 10 PH7 devices were run under identical test conditions. In Fig. 8 a typical PH7 and a typical NRF1 device are plotted and show an improvement in performance for NRF1 consistent with that shown during DC-HTOL.

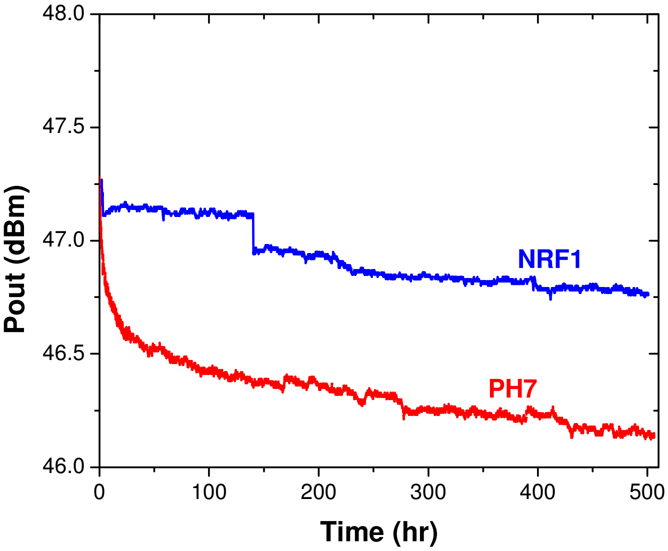

Figure 8: Comparison of RF-HTOL results for PH7 and NRF1.

V. CONCLUSION

Nitronex's NRF1 technology has shown excellent reliability performance as characterized by 3-temperature DC lifetest, DC-HTOL, and RF-HTOL. The technology has shown an activation energy of 2.0eV with 20-year drift rates of less than 3% in maximum drain current when operated at 150°C. Additionally when compared with the previous PH7 technology improvement is seen in all areas of reliability. These results demonstrate continuous improvement in GaN reliability performance, and validate the release of the NRF1 technology as a qualified process platform.

REFERENCES

[1] S. Singhal et al, "Reliability of Large Periphery GaN-on-Si HFETs." Paper presented at Reliability of Compound Semiconductors Workshop 2005, Palm Springs, CA., 2005.

[2] B. Therrien et al, "A 36mm GaN-on-Si HFET Producing 368W at 60V with 70% Drain Efficiency." Paper presented at the 2005 IEEE International Electron Devices Meeting (IEDM), Washington, DC, 2005.

[3] S. Singhal et al, "GaN-on-Si Failure Mechanisms and Reliability Improvements." Paper presented at the 2006 IEEE International Reliability Physics Symposium (IRPS), San Jose, CA., 2006.

[4] S. Singhal et al, "Reliability of large periphery GaN-on-Si HFETs," Microelectronics Reliability, Volume 46, Issue 8, August 2006, pp. 1247-1253.