RELIABILITY OF LARGE PERIPHERY GAN-ON-SI HFETS

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ABSTRACT

GaN devices exhibit excellent potential for use in many RF applications. However, commercial acceptance of the technology has been hindered by the scarcity and non-statistical nature of the reliability results to date. In this work we present a full device level reliability study on GaN-on-Si HFETs developed at Nitronex with optimized materials growth, wafer fabrication, and device design. Reliability results on this technology include 3-temperature DC data that show an activation energy of 1.7eV and a MTTF > 10^7 hours at 150°C. Additionally, long duration DC-HTOL (30,000 device hours) and RF-HTOL (4,000 device hours) results demonstrate a repeatable low drift process. Finally, environmental tests such as autoclave and ESD demonstrate the ruggedness of the material system and technology.

I. INTRODUCTION

In the past several years GaN has progressed from a lab technology exhibiting high power densities on small periphery devices to a viable commercial technology showing repeatable high total power results on large periphery packaged devices [1,2,3]. The remaining challenge, before GaN devices can see significant product insertion, is demonstration of good reliability. In this paper we present a complete device level reliability dataset on Nitronex's baseline technology. The results show GaN-on-Si reliability levels meet or exceed those of many established technologies.

II. BACKGROUND

Devices reported in this work are for undoped $Al_{0.26}Ga_{0.74}N$ heterostructures grown on high resistivity Si (111) substrates by metal organic chemical vapor deposition (MOCVD). The process includes Ni/Au gates and Ti/Al/Ni/Au ohmic contacts. Source and drain fingers are plated with Au and airbridges are used for source connection. Devices are passivated and encapsulated with SiN_x. All devices in this study have a gate length of 0.7µm, gate-to-source spacing of 1µm, and gate-to-drain spacing of 3µm. Detailed descriptions of the process have been provided elsewhere [1,2].

All results reported in this work are taken from 36mm AlGaN/GaN HFETs with unit gate width of 200µm and gate pitch of 30µm. A picture of this 36mm device is shown in Fig 1. The devices come from Nitronex's baseline manufacturing process, which has demonstrated the ability to produce repeatable devices [1].

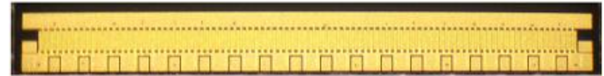
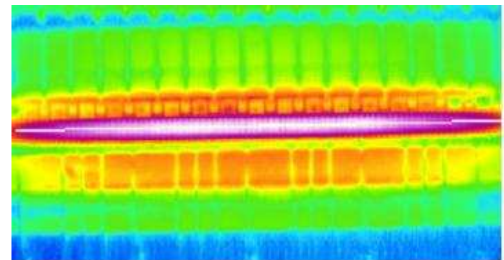


Figure 1: Picture of 36mm die consisting of 180 gate fingers with 200um unit gate width and 30um gate pitch.

For this reliability study, six wafers were selected randomly out of a 150-wafer baseline distribution and subjected to an extensive battery of tests. Over 400 die were used to generate the dataset described in this study. The test vehicle consisted of a transistor die attached to a high thermal conductivity CuW single-ended, ceramic packages using a AuSi eutectic process. The sources were grounded to the package base through backside vias in the 150µm-thick silicon wafer. Internal matching networks were used to transform both the input and output to higher impedances. These devices typically deliver 60-70W of CW saturated output power along with 60-65% efficiency at an operating voltage of 28V and frequency of 2.14GHz [4]. Prior to life testing, IR imaging was used to characterize 42 devices to validate junction temperature (T_j) calculations. A typical thermal image and the distribution plot of T_j for all devices are shown in Fig 2. The thermal resistance from these measurements is used in all lifetest calculations.



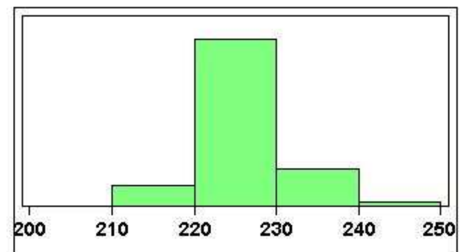


Figure 2: Thermal image of typical device (top) and distribution plot from 42 devices (bottom). All device biased at 28V and 2.3A.

III. Results & Discussion

The philosophy for this initial round of testing was to focus on reliability of the intrinsic device and gain insight into associated failure mechanisms. The testing can be divided into 3 major categories: DC, RF, and environmental testing. DC testing consisted of a 3-temperature life test to determine activation energy and a 200°C High Temperature Operating Life (HTOL) test to provide a significant number of device hours under accelerated operating conditions. RF testing focused on lifetests designed to confirm that the RF operation did not introduce failure mechanisms different from those seen in the DC portion of the testing, as well as survivability (high VSWR) testing. Environmental testing included humidity resistance and ESD testing. Results in each of these areas are presented below.

A. DC Testing

In DC-HTOL testing, devices are stressed at the DC operating voltage and maximum junction temperature for extended periods of time. For this study devices were stressed at 28V and 200C using a custom built HTOL test rack capable of simultaneously stressing 100 devices. This test methodology has been used over the past 3 years to systematically study several process generations. All test runs have been at the aforementioned 28V and 200°C with stress times ranging from 1000 hours to 2000 hours. In total more than 125 devices have been tested and over 150,000 device hours of DC-HTOL testing have been accumulated. Test runs are described in more detail in Table 1 below.

Table 1: Description of historical DC-HTOL tests.

Completion Date	Device Size	No. Wafers	No. Devices	Stress Time	Device Hours
Q2 2003	2mm	3	18	2,000 hrs	36,000 hrs
Q1 2004	16mm	5	50	1,500 hrs	75,000 hrs
Q2 2004	16mm	2	10	1,000 hrs	10,000 hrs
Q4 2004	36mm	2	20	1,000 hrs	20,000 hrs
Q1 2005	36mm	5	30	1,000 hrs	30,000 hrs

This work focuses on results of DC-HTOL testing from the most recent generation of baseline devices described in section II. Thirty devices were randomly selected from 5 different wafers and placed under HTOL stress for 1,000 hours each (30,000 device hours). The stress condition was Vd=28V, Id=2.3A, T_j=200°C. The HTOL rack uses water-cooling to maintain a baseplate temperature of 30°C and the current of 2.3A was chosen (from the thermal imaging data) to produce a temperature rise of 170C above the baseplate temperature resulting in a T_j of 200°C. Prior to lifetest all devices went through a 24-hour DC burn-in. The burn-in is necessary to screen for infant mortality and to stabilize the device. Fig. 3 demonstrates the stabilization of the junction temperature obtained through the burn-in process. The drain current drop, and hence the accompany temperature drop, is compensated for with a readjustment of the drain current. Following the readjustment the junction temperature remains relatively constant.

Devices undergo a full battery of DC and RF characterization prior to the lifetest and this characterization is repeated at several intervals throughout the test. In this case devices were removed from the HTOL rack after 24, 168, 500, and 1000 hours of stress. At each of these downpoints, the full battery of DC and RF testing was repeated. Box plots of the saturated drain current (Idss) versus test interval are shown in Fig. 4 and reveal tight distributions and a lognormal dependence between drift and time.

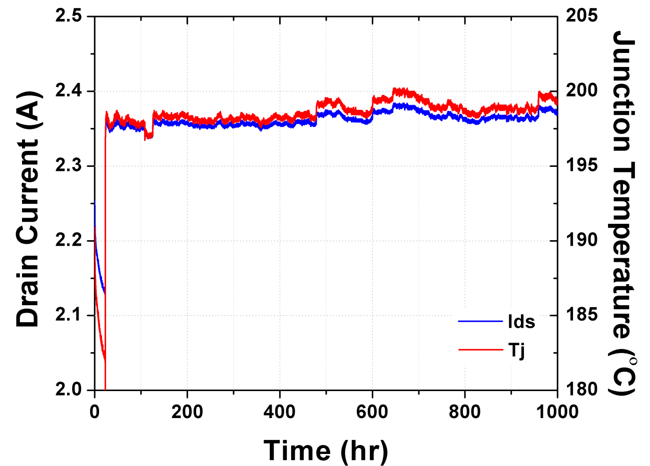


Figure 3: Plot of Id and T_j versus time for DC-HTOL test. T_j is readjusted after burn-in and remains constant.

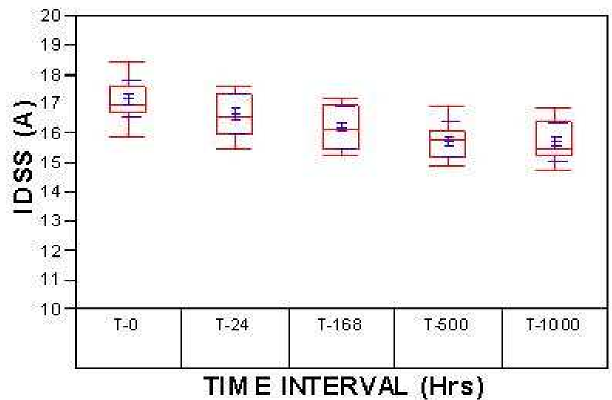


Figure 4: Box plots showing Idss versus time from DC-HTOL test.

A 3-temperature DC test was also performed to complement the DC-HTOL test. This test is less statistical, but is designed to determine a temperature acceleration factor. It is generally assumed that semiconductor devices follow an Arrhenius relationship with drift and temperature and the acceleration factor can be expressed as activation energy, Ea. Once again a custom test setup was used to stress the devices. The setup consisted of an oven with in-situ thermocouple feedback loop to control the ambient temperature. Junction temperatures of 260°C, 285°C, and 310°C were used for the test. The bias conditions were identical to the conditions used for the DC-HTOL test, Vd=28V and Id=2.3A. At each condition, 4-8 devices were stressed with the stress times ranging from 500 hours to 1000 hours. The in-situ drain current was measured at two-minute intervals to monitor the drift during the stress. Full DC and RF testing was only performed at the beginning and end of the test due to the difficulty in removing the parts from the oven

Fig. 5 shows the in-situ drain current versus time for a typical device from each of the 260°C, 285°C, and 310°C stress conditions in the 3-temperature test. Additionally the 200°C stress condition from the DC-HTOL test is shown. The results demonstrate the expected increase in drift with increasing temperature. A failure criterion of 15% drift is used and the data is extrapolated to determine a MTTF (mean time to failure) for each temperature group. The resulting MTTFs are plotted on an Arrhenius plot in Fig. 6, revealing an Ea of 1.7eV. Inclusion of the lower temperature 200°C results from the DC-HTOL test provides greater confidence that additional low activation energy mechanisms are not present in this process. Assuming a constant Ea, an extrapolation to a more traditional operating temperature of 150°C results in a MTTF $>10^7$ hours or a FIT <100. These numbers compare favorably to existing technologies such as Si-LDMOS and GaAs pHEMTs. [5,6,7].

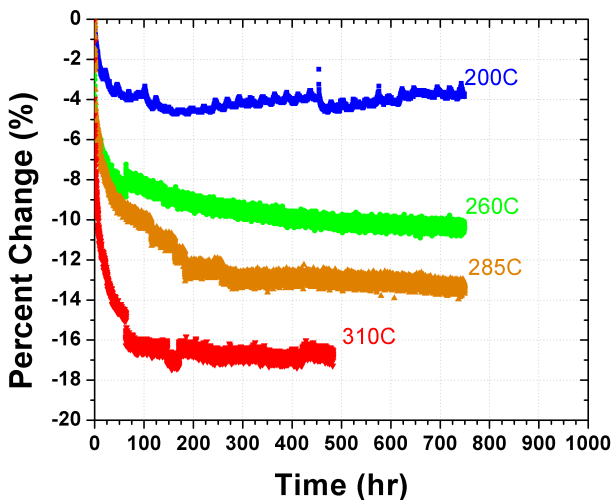


Figure 5: Drain current versus time for typical devices from 200°C, 260°C, 285°C, and 310°C DC stress test.

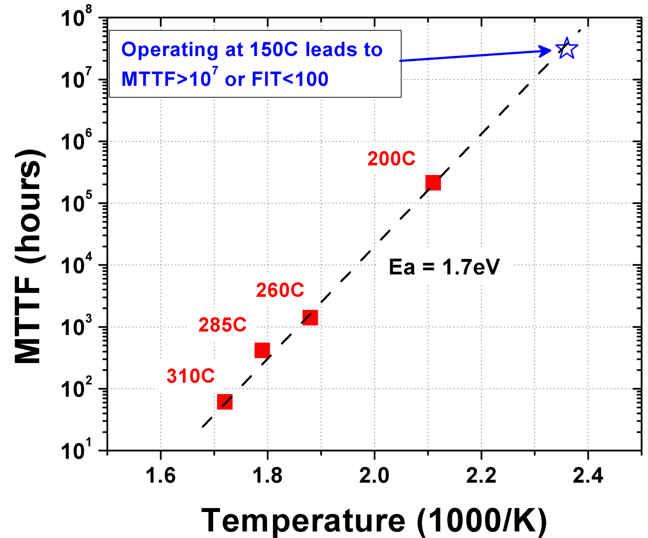


Figure 6: Arrhenius plot showing Ea=1.7eV and MTTF > 10^7 hours at 150°C.

Further analysis can be performed on the DC test results to predict the long-term drift over 20 years. For instance, the DC-HTOL results in Fig. 3 exhibit a lognormal dependence between drift and time. This lognormal fit can be extended out to 20 years (175,200 hours) and predict the long-term drift at 200°C. Additionally one can use the Ea previously determined and apply an acceleration factor to predict performance closer to the use temperature of 150°C. Applying these extrapolations to the DC-HTOL test results in 20-year drift rates of 14% at 200°C and 5% at 150°C, as demonstrated in Fig. 7.

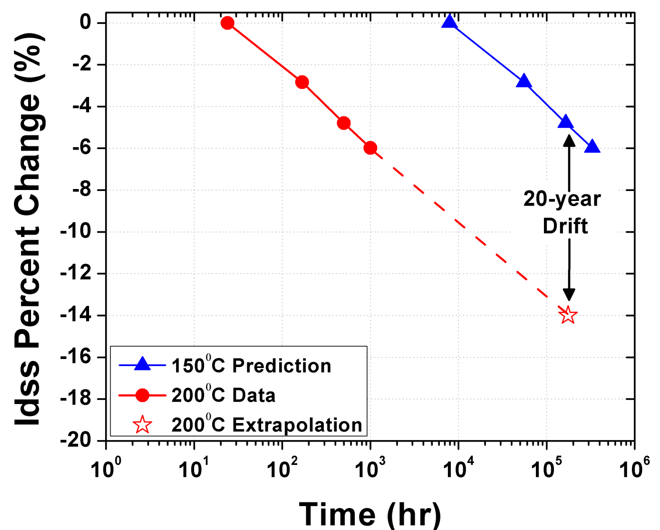


Figure 7: Extrapolation of 200°C DC-HTOL data demonstrating 20-year drift of 14% and 150°C prediction demonstrating 5% drift.

B. RF Testing

RF life testing was performed by way of a RF-HTOL test. Testing conditions were designed to be similar to those used for DC-HTOL (28V, 200°C) with the addition of RF input power sufficient to drive the device into 3dB compression. Eight devices were stressed for 500 hours each. The RF stress was performed at Naval Surface Warfare Center in Crane, IN. The devices were placed in a 50-ohm application board with flange temperature adjusted to provide T_j of 200°C (flange temperature ~80-100°C). Once again an adjustment was made in the first 24 hours to ensure that the temperature remained ~200°C throughout the test. In-situ monitoring of the output power was used to track degradation.

Fig. 8 shows all 8 devices have similar trends with lognormal dependence between output power drift and time. Extrapolating the curve to 20 years predicts a long-term drift rate of 0.9dB at 200°C. Plotting the output power drift (in watts), from the RF-HTOL test, and the drain current drift, from the DC-HTOL test, reveals a similar percentage drift versus time, as seen in Fig. 9. The similar lognormal dependence and overall drift rates between DC and RF stress testing suggests that the DC stress testing is sufficient for predicting device reliability.

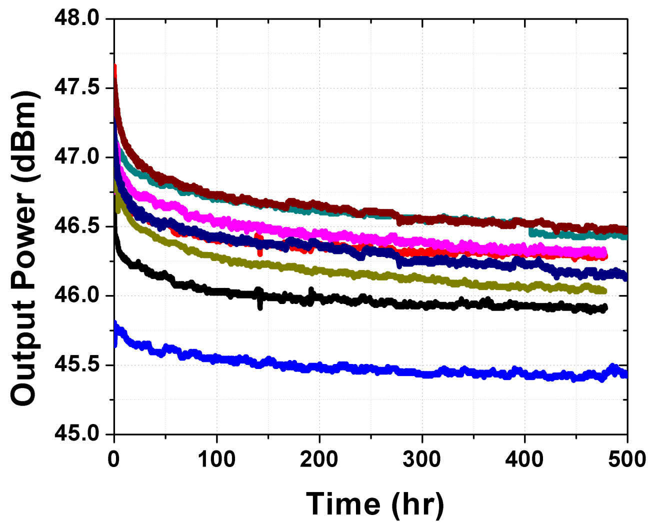


Figure 8: RF-HTOL results depicting output power versus time.

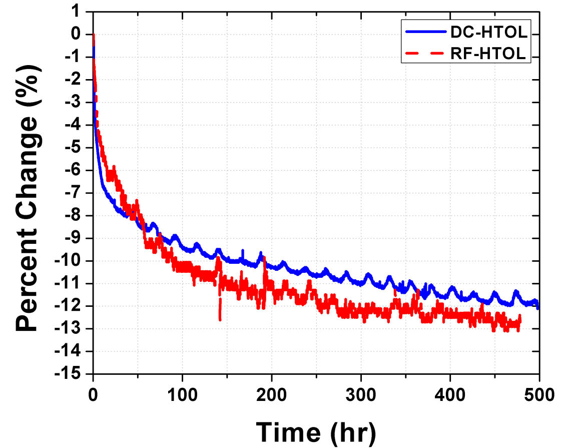


Figure 9: Comparison of drift from DC-HTOL and RF-HTOL test demonstrating similar performance.

Additionally, ruggedness testing was performed using a VSWR (voltage standing wave ratio) mismatch test. VSWR testing was performed by terminating the output of the application board with attenuation and a short. A 1dB attenuator and a short were used for 5:1 VSWR, while no attenuation and a short were used for 10:1 VSWR. In each case a line stretcher was used to sweep the impedance through all phases under the mismatch condition. Devices went through full DC and RF characterization before and after VSWR stress. A total of 10 devices were stressed under both VSWR mismatch conditions and all devices survived testing, with minimal changes in parametric performance. Results for 60V drain leakage (Vg=-8V, Vd=60V) and output power can be seen in Fig. 10.

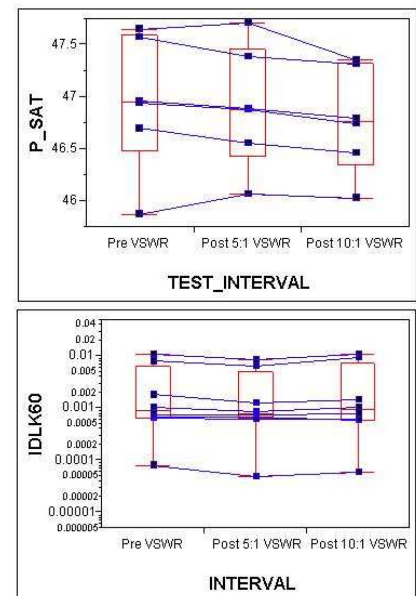


Figure 10: VSWR results show minimal change in output power (top) and 60V drain leakage (bottom) after 5:1 and 10:1 VSWR applied.

C. Environmental Testing

Finally, a battery of environmental tests was carried out on packaged parts. This included autoclave testing, temperature cycling, and ESD testing. The autoclave testing was carried out at 121°C, 100%RH (relative humidity), 15psi for 96 hours on 20 devices. The results, summarized in Fig. 11, showed no appreciable degradation. Temperature cycling was not performed on this generation of devices but results from previous generations showed no significant change in performance with similar packaging techniques after 250 cycles at –65°C to 150°C. Visual inspection following the autoclave and temperature cycling test showed no signs of delamination or other physical changes.

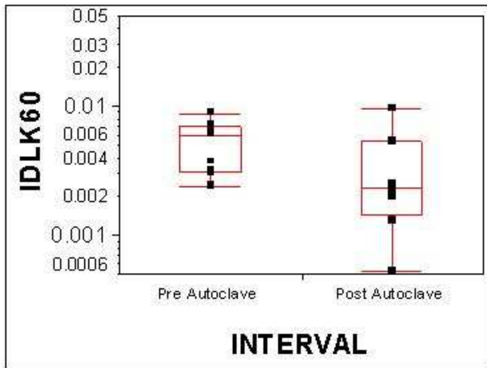


Figure 11: Results of Autoclave test showing minimal change in 60V drain leakage after 96 hours of stress (121C, 100%RH, 15psi).

Electrostatic Discharge (ESD) testing was carried out under both human body model (HBM) and machine model (MM) conditions. All pin combinations and polarities were stressed on 30 devices, with failure defined as a 10x increase in 60V drain leakage current. The results are shown in Fig. 12 and 13. Under HBM conditions all devices survived 1000V (class 1C) of stress, with only 1/30 devices failing at 2000V. Under MM conditions all devices survived 250V (class M3), and only 7/30 devices failed at 400V.

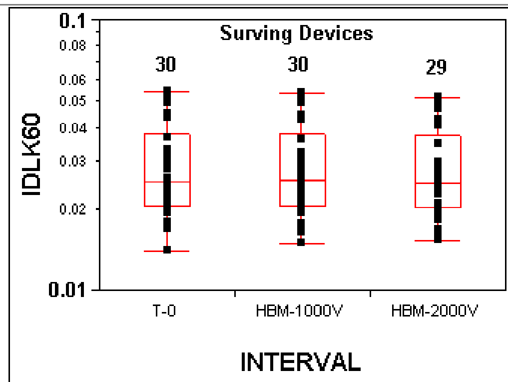


Figure 12: Results of HBM ESD test demonstrating no failures at 1000V and 1 failure at 2000V.

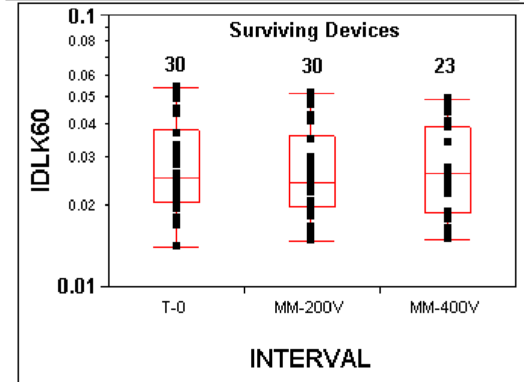


Figure 13: Results of MM ESD test demonstrating no failures at 200V and 7 failures at 400V.

V. Conclusion

Excellent results have been obtained in terms of DC, RF, and environmental reliability. Accelerated DC lifetests reveal an Ea of 1.7eV with a MTTF of $>10^7$ hours and a predicted 20-year drift rate of ~5% at 150C. Testing done under RF stress reveal similar drift rates. These results establish Nitronex's baseline GaN-on-Si reliability as being equivalent to that of existing technologies and demonstrate the viability of the technology as a manufacturable and reliable platform.

References

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