Qualification and Reliability of a GaN Process Platform

S. Singhal, A.W. Hanson, A. Chaudhari, P. Rajagopal, T. Li, J.W. Johnson,
W. Nagy, R. Therrien, C. Park, A.P. Edwards, E.L. Piner, K.J. Linthicum, I.C. Kizilyalli

Nitronex Corporation, 2305 Presidential Drive, Durham, NC 27703
Phone: (919) 807-9100; Fax: (919) 807-9200; E-mail: ssinghal@nitronex.com

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Abstract

In this paper, the qualification of a production GaN process platform is discussed. Details of the process repeatability, reliability and qualification methodologies are covered in detail. Additionally, concurrent product development efforts are also described. Reliability results include three-temperature DC testing that resulted in an activation energy of 2.0eV and DC-HTOL testing demonstrating 20-yr drift rates of less than 3% when operated at 150°C.

INTRODUCTION

Power transistors based on AlGaN/GaN have emerged as an attractive technology for high-power amplification in both commercial and defense applications [1, 2]. Until recently, marketplace acceptance of this new technology was limited in part by lack of a comprehensive reliabilty data set, and the perception of relatively immature manufacturing capabilites. In this paper we describe our first production-ready process, NRF1, and provide details of the qualification methodology followed. Specifically, reliability results are presented that include three-temperature life testing, DC-HTOL, RF-HTOL, ESD, VSWR robustness, autoclave, and temperature cycling. Details of product development are also given that demonstrate the high-performance and across-process repeatability obtained.

PROCESS

The NRF1 process makes use of a 100mm GaN-on-Si epitaxial process and includes a 0.5µm gate length fabrication process [3, 4]. The initial phase of the qualification process included running more than 50 wafers to establish typical performance levels and preliminary specification limits for the process. After successful processing of these 50 wafers, the NRF1 process platform was adopted for pre-production release in October of 2005. Full qualification was accomplished by September of 2006. In this period of time, more than 300 production wafers were fabricated to support product development and qualification efforts.

All NRF1 wafers are subjected to DC and RF tests at two distinct test points during the wafer fabrication process. The first following gate electrode formation, and the second following completion of front end of line processing. A list of pass/fail specifications is given in Table 1. A wafer must pass all specification limits to be considered spec-compliant and viable for product usage.

Table 1: NRF1 Specification Limits for inline testing.

Parameter	Description	Units	LSL	TGT	USL
BVDG	Two Terminal Off-State Breakdown Voltage	V	135	160	-
BVDS	Three Terminal Off-State Breakdown Voltage	V	95	130	-
GMX	Maximum Extrinsic Transconductance	mS/mm	250	290	330
IDLK_100	Drain Leakage	mA/mm	-	0.2	1.0
IDMAX	Maximum Open Channel Current	mA/mm	760	830	900
LOG_ISO	Isolation Leakage Current - LOG10	Log(A)	-	-9	-8
RC_TLM	Contact Resistance	Ohm mm	-	0.38	0.55
RDON	On Resistance	Ohm mm	2.4	3.0	3.6
RSH_CRBME	Epitaxial Layer Sheet Resistance	Ohm/sq	440	490	530
VP	Pinchoff Voltage	V	-1.50	-1.25	-1.00
NPSAT_W_MM	Saturated Output Power	W/mm	3.4	3.9	-
DEFF_MAX	Maximum Drain Efficiency	%	57	62.5	-

A trend chart for maximum drain current is shown for all NRF1 lots in Fig. 1. Each lot contains 4-7 wafers, thus giving the 300+ total wafers. The lots highlighted in blue signify those used for reliability and qualification activity and were sampled randomly across process.

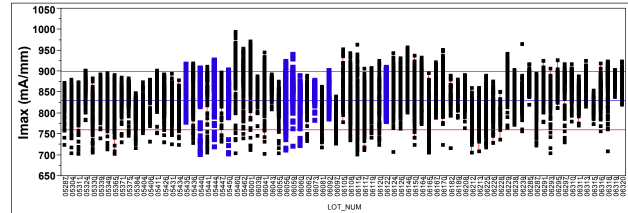

Figure 1: Trend Chart for Imax across process lot. Each lot represents 4-7 wafers.

PRODUCT DEVELOPMENT

After process consistency was established, the NRF1 platform was used to launch five commercial products. Three designed for the emerging WiMax market (NPT35015, NPT35050, and NPT25015) and two designed to provide broadband power for a number of general uses (NPTB00025 and NPTB00050). The first product released was the NPT35050 device in September of 2006. The NPT35050 consists of a transistor die attached into a high thermal conductivity CPC single-ended, ceramic package using a AuSi eutectic process. During product development devices were built from numerous NRF1 wafers, highlighted in Fig. 1. This was done to ensure that both the internal matching network and 50-ohm application board gave consistent performance across process. Typically, these devices produce 60-70W of saturated CW power at an operating voltage of 28V and frequency of 3.5GHz, demonstrated in Fig. 2.

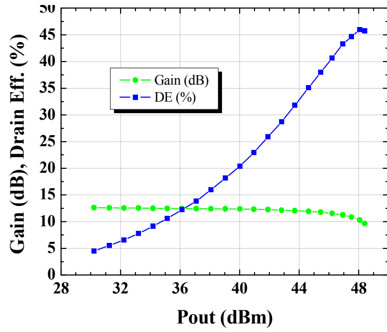

Figure 2: CW performance of NPT35050 Device.

The WiMax performance of the NPT35050 is measured under an OFDM modulated signal. The part delivers 2.5% EVM, 18% efficiency, and 11dB Gain at an output power of 6W and over the large operating bandwidth of 3.3 to 3.8GHz as shown in Fig. 3.

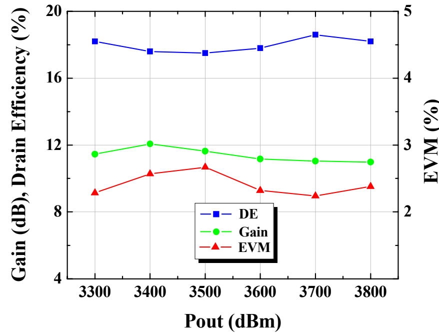

Figure 3: OFDM performance as a function of frequency,

After collecting the performance characteristics from multiple devices across several process lots, a final production test plan was released with final specification limits derived from the across-process variation. Numerous devices have been manufactured and tested to this plan and a distribution for Gain at 3.6GHz for over 1,500 devices from multiple process lots is shown in Fig. 4.

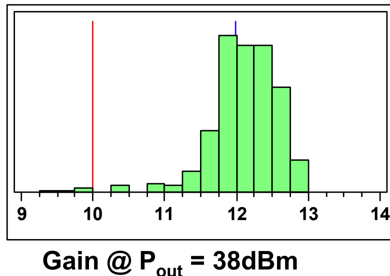

Figure 4: Distribution of Gain at 3.6GHz and P_{out}=6W for over 1,500 NPT35050 devices.

The final piece to the product development was developing circuit models for the NRF1 devices. So far compact models have been developed using both a proprietary version of the Curtice model and publicly available version of the Angelov model [5].

RELIABILITY TESTING

Following process and product development, an extensive reliability evaluation was performed. The reliability evaluation was divided into three phases; intrinsic technology tests, product device tests, and product assembly tests. Intrinsic testing focused on validating the basic NRF1 GaN technology by performing fundamental tests such as three-temperature DC lifetests. The product device tests focused on electrical testing specific to the product and included DC-HTOL, ESD, thermal imaging, etc. Finally the product assembly level tests focused on packaging aspects such as autoclave, temperature cycling and thermal shock. The NPT35050 served as the technology qualification vehicle for the NRF1 process and was used in all tests listed above. Devices from a minimum of three process lots were used in all reliability testing.

Prior to any life testing, the thermal performance of the device was characterized to ensure proper junction temperature calculations. Thermal impedance was measured using a QFI Infrascope II infrared thermal imaging microscope. The measurement was made with a heat sink temperature of 80°C and a thermocouple mounted below the package to measure the case temperature. The bias condition was V_{DS}=28V and I_{DS}=975mA for each device, which is equal to the power dissipated under the RF operating point of Pout=6W and Efficiency = 18%. A total of 8 samples were measured from 3 wafers. Table 2 summaries the results on the 8 devices and demonstrates a consistent thermal performance across process.

Table 2: Summary of Thermal Resistance measurements.

DUT	T_{case} (°C)	$T_{junction}$ (°C)	R_{TH} (°C/W)	Pass/Fail
1	88.50	142.00	1.95	PASS
2	89.80	143.00	1.95	PASS
3	88.90	137.00	1.76	PASS
4	88.10	134.00	1.68	PASS
5	88.60	141.00	1.92	PASS
6	88.00	137.00	1.79	PASS
7	88.20	136.00	1.75	PASS
8	88.20	141.00	1.93	PASS
AVG	**88.54**	**138.88**	**1.84**	
STD DEV	**0.59**	**3.27**	**0.11**	

Three-temperature DC testing was carried out in order to determine the activation energy for the NRF1 process. Testing consisted of DC stress at V_{DS}=28V and I_{DS}=2.34A with ambient temperature adjusted to achieve junction temperatures of 260°C, 285°, and 310°C. For each stress temperature 25-30 devices were tested with stress time ranging from 400 to 1000 hours. A failure criteria of 15% drift of in-situ drain current was used. Failures followed a lognormal distribution and cumulative failure plots were used to assess the MTTF for each temperature group, as shown in Fig. 5.

In Fig. 6, the MTTF for each temperature is plotted on an Arrhenius plot and reveals an activation energy of 2.0eV for the NRF1 process platform. When this curve is extrapolated to a typical use temperature of 150°C, a MTTF greater than 10^7 hours is predicted.

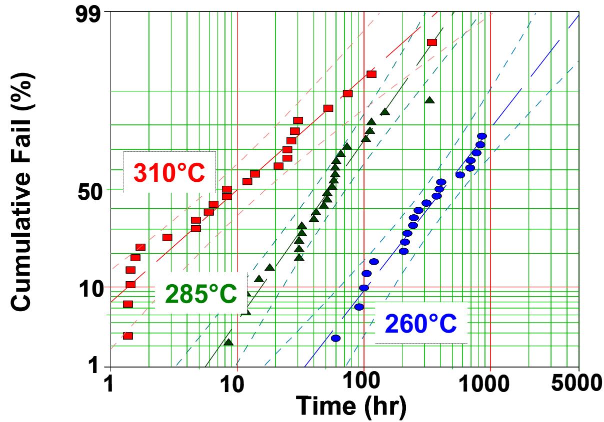

Figure 5: Cumulative failure plots with 90% confidence intervals.

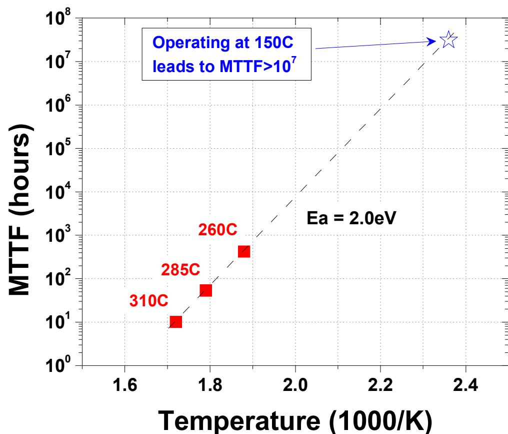

Figure 6: Arrhenius Plot showing activation energy of 2.0eV and MTTF > 10^7 hours at 150°C.

DC-HTOL testing was carried out at V_{DS}=28V and T_J=200°C for 2000 hours. A 45 piece sample was placed under DC-HTOL stress, with results shown in Fig. 7 for maximum drain current (Imax). The box plots show consistent performance between the 45 samples and minimal drift with time. Figure 8 is used to predict the long term drift rate. In this figure each of the red dots represents the median for the 45 samples at the test downpoints of 0, 36, 168, 500, 1000, 1500, and 2000 hours. The data is fit to a logarithmic relationship versus time and extrapolated forward to 20-years of operation showing a drift of <7% in maximum drain current under 200°C operation. The previously determined activation energy of 2.0eV can be used to calculated an acceleration factor and predict the drift at a more typical operating temperature of 150°C. This 150°C drift is seen in the blue curve and shows <3% drift over 20 years.

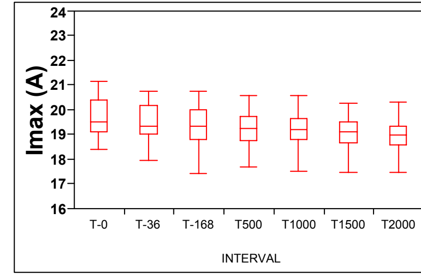

Figure 7: DC-HTOL results for maximum drain current versus test interval out to 2000 hours.

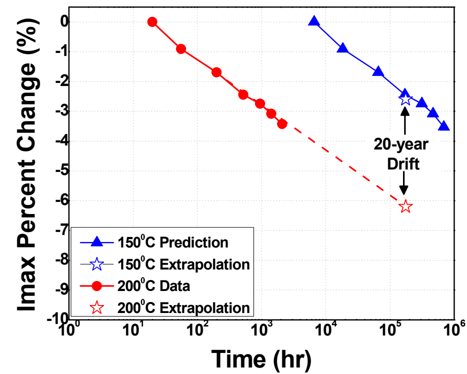

Figure 8: DC-HTOL results measured at 200°C (red) and converted to 150°C (blue) showing drift out to 20-years.

RF-HTOL testing was carried out in order to verify that the RF stimulus did not induce additional failure mechanisms. A total of 6 samples were stressed at V_{DS}=28V, Freq=2.14GHz, and RF input power sufficient to drive the device into 3dB gain compression (P_{out}~50W) with the baseplate adjusted to produce a T_J=200°C. Fig. 9 shows the drift in the in-situ Pout versus time for the 6 samples.

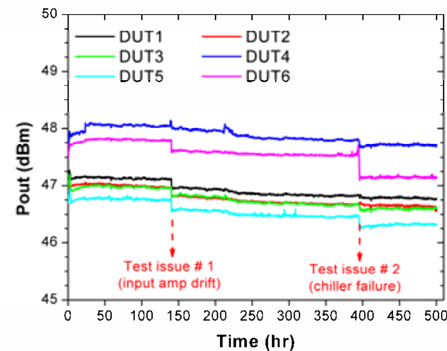

Figure 9: RF-HTOL results on 6 samples at V_{DS}=28V, P_{out}~50W, and T_J=200°C.

There were two test issues which lead to systematic shifts in the data. The first issue occurred around 130 hours and was a drift in the input amplifier causing the input power to drop ~0.25dB. The second issue occurred at 388 hours and involved a chiller failure which caused the junction temperature to rise significantly before the devices were powered down. Some devices experienced junction

temperatures as high as 400°C for 10-20 minutes. After resetting the junction temperature all devices came back to within 0.2dB of original value except DUT 6 which lost about 0.5dB in performance.

ESD testing was carried out using the both the HBM and MM waveform on 3 devices each from 3 different wafers. Each pin combination (-GS, +GS, -GD, +GD) was stressed with 3 test pulses and full DC characterization was performed before and after stress. Figure 10 shows results after a HBM voltage stress of 500V and 1000V. No damage was seen after 1000V, leading to a HBM classification of 1C. Figure 10 also shows results after a MM voltage stress of 100V and 200V. No damage was seen after 200V, leading to a MM classification of M3.

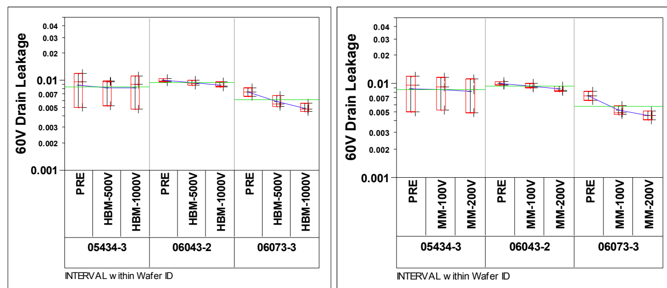

Figure 10: 60V Leakage measurements shown before and after ESD stress with both HBM (left) and MM (right) stimulation.

Robustness of the devices was furthered tested by way of a VSWR mismatch test. VSWR mismatch was presented to devices under operating conditions of V_{DS}=28V, I_{DQ}=750mA, P_{out}=6W and Frequency=3.5GHz with OFDM modulation applied. A total of 5 devices were stressed and characterization before and after stress shows no significant shift in performance as seen in Fig. 11.

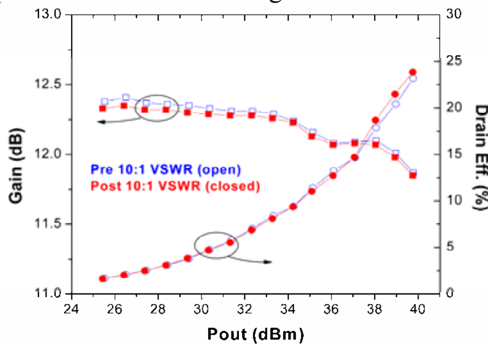

Figure 11: RF power sweep for typical device before and after stress with 10:1 VSWR mismatch.

A number of environmental tests were also performed including autoclave, temperature cycling, and thermal shock. Autoclave was carried out at 121°C, 15psi, 100%RH for 96 hours with no failures after stress. Temperature cycling was carried out with air-to-air cycles from -65°C to 150°C with 500 cycles. Once again no degradation in electrical performance was seen. Furthermore, C-SAM measurements were used to evaluate the die attach before and after stress. Figure 12 reveals no voids or cracking caused by the temperature cycling.

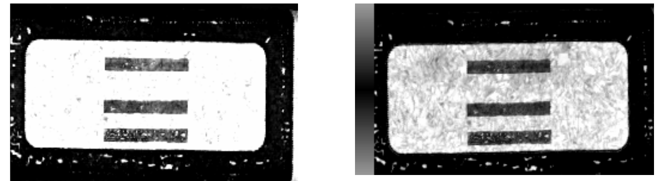

Figure 12: C-SAM figures revealing no change in die attach before (left) and after (right) temperature cycling.

Finally, thermal shock was performed with liquid-to-liquid cycling from -55°C to +125°C with no degradation seen on any devices. The mechanical integrity of the package was evaluated by tests such as mechanical shock, vibration, solderability, etc.

CONCLUSIONS

Details on the qualification of the NRF1 process platform have been described. Process maturity was demonstrated allowing for development of high-performing and repeatable product devices. These product devices were put through an extensive reliability qualification. Reliability results included a high E_a of 2.0eV with a corresponding high MTTF of > 10^7 hours at 150°C. Good drift characteristics were also shown via HTOL tests under both DC and RF stimulus. Finally robustness was demonstrated with ESD and VSWR mismatch testing.

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ACRONYMS

GaN: Gallium Nitride
HBM: Human Body Model
HTOL: High Temperature Operating Life
MM: Machine Model
MTTF: Mean time to Failure