Performance of AlGaN/GaN HFETs Fabricated on 100mm Silicon Substrates for Wireless Basestation Applications

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***Abstract* — Third generation wireless communications standards such as W-CDMA place challenging requirements on microwave power transistors. To date, these challenges have been addressed with two primary technologies, Si LDMOS FETs and GaAs FETs. A new technology (AlGaN/GaN HFET) that shows the potential for addressing these strict system requirements is now becoming available. The growth and fabrication of GaN-based HFETs on a manufacturable 100mm silicon platform are discussed. Results from 36mm GaN HFETs are reported with particular attention to their ability to address the needs of the W-CDMA base transceiver station output power stage, demonstrating in excess of 15W output power at W-CDMA operation with –39dBc ACPR and 29% drain efficiency. Results of initial high-temperature operating life testing are presented, showing excellent device stability at a junction temperature of 200ºC, and predicting about 10% drift in DC parameters and less than 1 dB in output power over a 20-year life.**

***Index Terms* — W-CDMA, gallium nitride, RF power transistor, ACPR, reliability**

I. INTRODUCTION

W-CDMA basestations are a key element in the infrastructure for third generation (3G) wireless communications. There are demanding requirements on the output stage of the basestation in order to reliably deliver the required signal quality while keeping the operating cost of the system to a minimum [1]. The performance can be broken out into several important areas. These are: 1) total output power, 2) power gain, 3) signal linearity, and 4) system efficiency. The heart of the output stage is the power transistor, which is also the component that is critical in defining the system level performance. The high power requirement has thus far limited the selection of power transistors to only two main technologies, silicon based LDMOS FETs and GaAs FETs. This paper discusses GaN HFETs, grown on a manufacturable 100mm Si platform, as a new technology that has demonstrated the ability to meet the performance and cost requirements.

GaN and related alloys have been the focus of intense development efforts for the past decade. Many impressive results have been published for AlGaN/GaN HFETs on both sapphire and silicon carbide substrates [2, 3, 4]. More recently, work has been undertaken to develop this technology on silicon substrates, showing much promise [5, 6]. We have developed a patented technology known as Sigantic™ [7] that allows us to grow high quality GaN on silicon substrates. Using this technology and our 100mm GaN wafer fabrication facility, we have developed a power transistor technology designed specifically for the output stage of third generation wireless basestations. The following will demonstrate the performance of these high power transistors and will discuss how the requirements discussed above are addressed using this technology.

To be viable in commercial or military applications superior operational performance must be complemented by adequate reliability performance. There is currently very little literature on overall reliability of GaN technology. The majority of existing reliability studies on GaN focus on the reliability of individual components, such as ohmic or Schottky contacts [8, 9] or on hot electron induced stress in AlGaN/GaN HFETs [10], typically limited to small samples sizes at the laboratory level. Here we will present results of a first comprehensive high-temperature operating life test, predicting excellent 20-year life performance.

II. EXPERIMENTAL DETAIL

A. GaN Material and Fabrication

High quality GaN is epitaxially grown on 100mm silicon substrates by MOCVD (metalorganic chemical vapor deposition). This is facilitated by the growth of a stress mitigating transition layer preceding the growth of the GaN layer. The device structure is an undoped (Al, Ga)N based HFET with 20% AlN mole fraction in the barrier layer. The devices are fabricated using techniques that are typical for GaN-based devices, described in more detail elsewhere [11]. The results presented in this work are from a typical device selected from the baseline wafer growth and fabrication process. This process is designed to deliver consistency in device performance for samples

and amplifier development. Figure 1 shows the behavior of the wafer process as indicated by the variation of the maximum drain current both across a wafer and across the process. The wafer-to-wafer variability is less than 10% and the wafer uniformity is better than 5%. The maximum drain current has proven to be a good indicator for the important device performance parameters of interest. Thus, the uniformity observed here both across wafers and within each wafer indicates that the samples characterized for this work are typical and that similar results are observed on a large fraction of the chips delivered from this process.

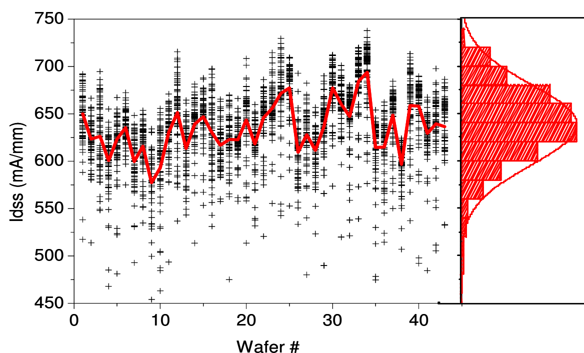

Figure 1: Wafer to wafer variability of maximum drain current over 43 wafers (69 datapoints per wafer)

B. Layout and Packaging of the Device

The device geometry characterized here has 36mm of total gate periphery. This is made up of eighteen 2mm unit cells each having ten 200µm wide gate fingers and a gate-to-gate pitch of 30µm. The device layout was designed for optimal tradeoff of capacitive loading and thermal dissipation. The thermal impedance of this device in a standard package is 2.0^{o}C/W, resulting in a modest junction temperature rise of 78°C at maximum W-CDMA power.

The chip is packaged into an industry standard high power device package containing a CuW baseplate to provide low thermal impedance for efficient power dissipation. The die is attached to the package base using a AuSi eutectic bonding process. No intentional impedance matching of the chip was done inside of the package; the matching network was implemented outside of the package, using either tuners or circuit board matching circuits. As will also be discussed below, all devices undergo a 24-hour burn-in at a junction temperature of 200°C following packaging, which stabilizes the device for long-term performance.

C. Measurements

Measurements were carried out in two configurations, a load-pull system and an application test board. Load-pull measurements were conducted at 2.14 GHz using a Focus Microwaves passive tuner system. For load-pull testing, the device was mounted in a test fixture that provided prematching via a tapered transmission line, with matching to 50 ohms done using the tuners. The test boards were impedance matched with surface mount shunt capacitors. Both the test fixture for the load-pull measurements and the test boards have bias networks that are designed for use with a modulated signal of the appropriate bandwidth.

The choice of operating conditions for these devices is key to delivering the desired performance. We have determined that the optimal conditions for single tone performance differ from those under W-CDMA modulation. The parameters that have a significant impact on the performance are: the quiescent bias current, the source impedance, and the load impedance.

III. RF-Results

The performance of the device with an unmodulated single-tone input is shown in Figure 2. The operating condition for this device was a quiescent current (I_{dq}) of 1000mA and a drain voltage (V_{ds}) of 28V. The device demonstrates 13.4dB of gain, in excess of 50% peak drain efficiency and a saturated output power of 55W.

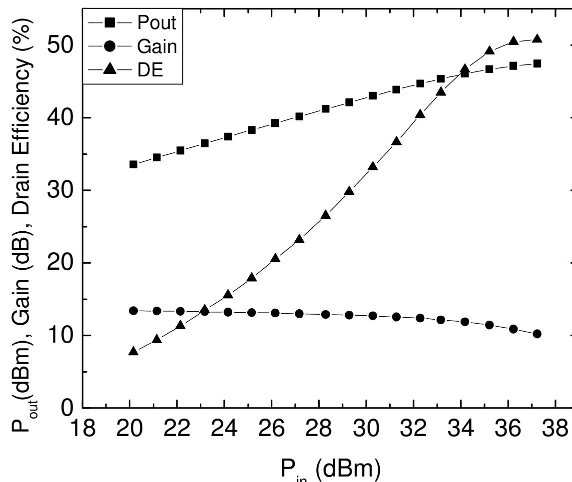

Figure 2: Output power characteristics of a 36 mm AlGaN/GaN HFET operated with single tone RF input at 2.14 GHz

Now we consider this device in the framework of W-CDMA operation. The performance-limiting factor for W-CDMA operation is typically the linearity of the device, which is often defined in terms of the adjacent channel

power ratio (ACPR). Once the limit on linearity is defined by the maximum allowed ACPR level, the other device characteristics are optimized to deliver the best possible performance. The device is biased and impedance matched specifically for the W-CDMA signal. In addition, the device must be operated well below the level of single-tone power saturation to accommodate the large peak-to-average ratio of the modulated signal. This may require that a device be backed-off as much as 10 dB below the saturated output power, simultaneously giving up as much as 40% of the device drain efficiency. This forces the designer to tradeoff the power/efficiency directly against the linearity of the device.

The total output power of the basestation is defined by the desired range of coverage and the traffic density, thus defining the number of power transistors needed. One would like to meet the total system output power requirements while minimizing the system complexity. GaN, with its higher intrinsic power density, makes it possible to produce devices of higher total power while remaining within some reasonable physical constraints for chip size.

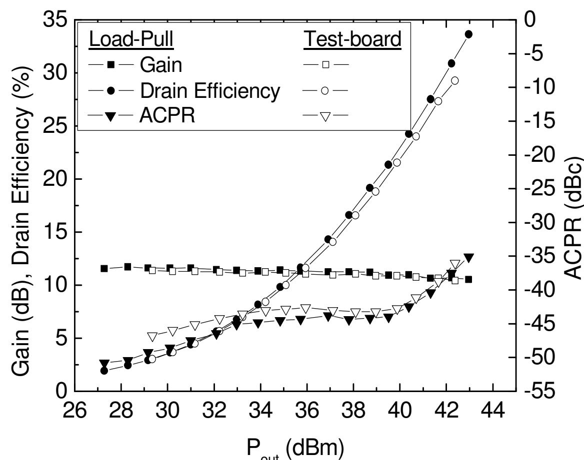

Figure 3: Output characteristics of an AlGaN/GaN HFET optimized for operation under W-CDMA modulation conditions. Measurement carried out in load-pull system(solid symbols) and in the RF test board(open symbols).

The device with single tone results shown above was re-optimized for W-CDMA operation based on the ACPR measured on the output of the device. The W-CDMA signal used was a single carrier 3GPP signal, corresponding to Test Model 1 with 64 users and 100% clipping (PAR of 9.8 dB @ 0.01%) [1]. The ACPR was measured with a 3.84 MHz channel bandwidth at an offset of 5 MHz from the center of the operating band. The quiescent conditions are the same as used for single-tone operation, but the source and load impedances have been modified. The results of a power sweep with these conditions are shown in Figure 3 versus output power. There are several points of interest on this plot. First, for output power levels below 40dBm, there is a plateau in the ACPR response versus output power, meaning that the ACPR requirement can be met over a wide range of power, assuming that the plateau is below the required maximum ACPR level. For a maximum ACPR level of –39dBc, the device shown in Figure 3 delivers a maximum output power and drain efficiency of 42dBm (15.8W) and 29%, respectively. Testing under the same operating conditions, but on an RF test board with external matching of the input and output impedances to 50 ohms, reveals almost identical performance as compared to the load pull results (open symbols in Figure 3).

The ability to deliver this relatively high power density (439mW/mm) leads to the simplification of the total packaged part, requiring fewer chips and matching components in the package.

IV. Burn-in and Reliability

Each wafer from the baseline production process is sampled for wafer acceptance testing. To date, more than 1500 devices have been sampled through this process, from more than 150 wafers over several product development generations. The standard procedure is to sample a minimum of five devices from each wafer. The sample is subjected to a 24-hour High Temperature Operating Life (HTOL) burn-in test. The HTOL test is performed using a custom built system capable of biasing up to 100 devices at a dissipated power level of 90W each. The HTOL system uses liquid cooling to maintain a base plate temperature of 22°C.

The bias point is chosen to achieve a power level that results in the desired junction temperature, Tj, for stress. For the 16mm devices used in the following, the R_{th} was determined to be 5°C/W, and the devices were biased at a quiescent current of 1.3A at 28V resulting in a Tj of 200°C. For comparison, the junction temperatures during W-CDMA operation and under CW conditions at saturation are 105°C and 155°C, respectively.

The burn-in test is intended to stabilize the device performance and to provide a first glimpse at the reliability behavior. The criteria for failure for a device during burn-in are either catastrophic (device burn out) or a change in any parameter greater than ±15%, or ±0.5dB (JEDEC JESD2, Transistor, Gallium Nitride Power FET, Generic Specification). For our GaN devices, burnout while under bias has been non-existent.

Using the same setup as described above, a 1500-hour HTOL test has been performed on 45 devices of 16mm gate periphery. The samples were taken from five wafers representing three different process lots. One device from each wafer was used as a test control. All 45 devices survived the test. The means for each parameter from the 24-, 48-, 168-, 500-, 1000- and 1500-hour test down-points have been fit to log curves. As an example, the results for I_{DSS}, and P_{sat} are shown in Figure 4. Projecting the curves forward from 1500 hours to 20 years, we find that the DC parameters tested are expected to change less than 10% from 24 hours through 20 years. Similarly, the P_{sat} degradation is less than 1.0dB.

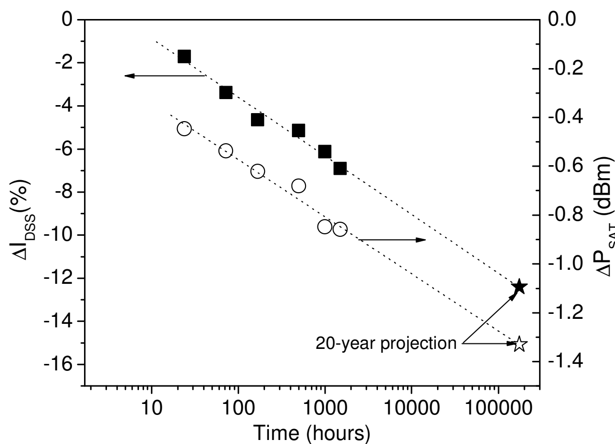

Figure 4: 200°C operating life test: Saturated current, and saturated RF power up to 1500 hours of operation, projecting excellent 20-year performance

V. CONCLUSIONS

A process for producing AlGaN/GaN HFETs on a manufacturable platform of 100mm silicon substrates has been described. Devices from this process have been selected and their performance tested under single-tone and W-CDMA modulation. The results show that both in the laboratory environment of a load-pull measurement system and in the more practical environment of a 50 ohm test board, these devices are capable of delivering power and efficiency levels that make them attractive for the W-CDMA application. In general the reliability of the device is encouraging, with projected parametric drift of less than 10% for DC and less than -1.0dB for P_{sat} over a 20-year lifetime, provided that the devices are burned in for 24 hours under DC bias prior to being deployed.

REFERENCES

[1] 3GPP Specifications for W-CDMA Basestations (http://www.3gpp.org/ftp/Specs/html-info/25141.htm)

[2] Y. Ando, Y. Okamoto, H. Miyamoto, N. Hayama, T. Nakayama, K. Kasahara, M. Kuzuhara, "A 110-W AlGaNGaN Heterojunction FET on Thinned Sapphire Substrate," *IEDM Technical Digest*, pp. 381-384, December 2001.

[3] J.W. Palmour, S.T. Sheppard, R.P. Smith, S.T. Allen, W.L. Pribble, T.J. Smith, Z. Ring, J.J. Sumakeris, A. W. Saxler,, and J.W. Milligan, "Wide Bandgap Semiconductor Devices and MMICs for RF Power Applications," *IEDM Technical Digest.*, pp. 385-388, December 2001.

[4] T. Kikkawa, M. Nagahara, N. Adachi, S. Yokokawa, S. Kato, M. Yokoyama, M. Kanamura, Y. Yamaguchi, N. Hara, K. Joshin, "High-power and high-efficiency AlGaN/GaN HEMT operated at 50V drain bias voltage", *2003 IEEE RF-IC Symposium*, pp. 167-170, 2003

[5] R. Behtash, H. Tobler, M Neuburger, A. Schurr, H. Leier, Y. Cordier, F. Semond, Fnatali, and J. Massies, *Electronics Letters*, Vol. 39 (7), pp. 626-628, April 2003.

[6] W. Nagy, J. Brown, R. Borges, S. Singhal, "Linearity characteristics of microwave-power GaN HEMTs", *IEEE Trans. on MTT*, Vol.51, No.2, Feb., 2003.

[7] Pradeep Rajagopal, Thomas Gehrke, John C. Roberts, J. D. Brown, T. Warren Weeks, Edwin L. Piner, and Kevin J. Linthicum, "Large-Area, Device Quality GaN on Si Using a Novel Transition Layer Scheme," Mat. Res. Soc. Symp. Proc., **743** (3), 2003.

[8] E. Monroy, F. Calle, T. Palacios, J. Sanchez-Osorio, M. T. Montojo, F. Omnes, Z. Bougrioua, I. Moerman, P. Ruterana, "Reliability of Schottky contacts on AlGaN", *Physica Status Solidi (a),* vol. 188 (1), pp. 367-370, 2001.

[9] J. Wuerfl, J. Hilsenbeck, E. Nebauer, G. Trankle, H. Obloh, W. Osterle, "Reliability of AlGaN/GaN HFETs comprising refractory ohmic and Schottky contacts", *Microelectronics Reliability,* vol. 40 (8-10), pp. 1689-1693, 2000.

[10] H. Kim, A. Vertiatchikh, R. M. Thompson, V. Tilak, T. R. Prunty, J. R. Shealy, L. F. Eastman, "Hot electron induced degradation of undoped AlGaN/GaN HFETs", *Microelectronics Reliability*, vol. 43 (6), pp. 823-827, 2003

[11] A. Vescan, J. D. Brown, J. W. Johnson, R. Therrien, T. Gehrke, P. Rajagopal, J. C. Roberts, S. Singhal, W. Nagy, R. Borges, E. L. Piner, K. J. Linthicum, "AlGaN/GaN HFETs on 100mm silicon substrates for commercial wireless applications", *Physica Status Solidi (c)*, 0, No.1, 52,2002.