

## SYMPOSIUM Y: GAN AND RELATED ALLOYS

### MOCVD AlGaN/GaN HFETs on Si: Challenges and Issues

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#### Abstract

AlGaN/GaN based high power, high frequency high electron mobility transistors (HEMTs) have been in development for over a decade. Although much progress has been made, AlGaN/GaN HEMT technology has yet to be commercialized. The choice of silicon as the substrate for the growth of GaN-based epi layers will enable commercialization of AlGaN/GaN based HEMTs, because of its maturity, scalability, reproducibility and economy. One of the epitaxial issues pertaining to the growth of AlGaN/GaN HEMTs on Si is the understanding of parasitic losses that can adversely impact the RF device performance. The effect of the III-N MOCVD process on the resistivity of the Si substrate, and correlations between the Si substrate resistivity and AlGaN/GaN HEMT RF characteristics are presented. Optimization of the MOCVD growth process led to a reduction in parasitic doping of the Si substrate. This resulted in the following improvements: (a) small signal gain increased from 17 to 21dB, (b) the cut-off frequency increased from 7 to 11GHz and (c) the maximum frequency of oscillation improved from 12 to 20GHz. This optimized process will enhance performance of AlGaN/GaN HEMTs at higher frequencies.

#### Introduction

Successful growth of high quality AlGaN/GaN high electron mobility transistors (HEMTs) on Si offers a pathway to commercialize GaN-based transistors for many applications, including those in the RF microelectronics area. As a result of this potential, several groups have focused attention to growth<sup>1, 2, 3</sup> of GaN-based epi layers on silicon substrates and the fabrication of various devices<sup>4, 5, 6, 7, 8</sup> thereof.

The resistivity of the Si substrate used to grow AlGaN/GaN HEMTs is an important parameter that impacts high frequency operation of the resultant power amplifiers. Highly resistive ( $\rho > 10^4$  ohm-cm) Si (111) substrates offer an effective platform for the growth and operation of high frequency of AlGaN/GaN HEMTs. A non-optimized MOCVD process can lead to the undesirable formation of a localized Al and Ga doped, p-type conductive layer in the Si substrate at the Si/III-N interface. We report on the development of an optimized MOCVD process that reduces the formation of the parasitic p-type layer at the Si/III-N interface. The dramatic reduction of the lossy parasitic p-type layer resulted in improved RF performance of AlGaN/GaN HEMTs on Si.

#### Experimental

The experiment consisted of two parts. In the first part, the effect of the growth conditions on the silicon substrate resistivity was monitored. In the second part, AlGaN/GaN HEMT devices were fabricated to correlate appropriate device performance parameters to the substrate

conductivity. In all cases, the substrate starting resistivity was  $> 10^4$  ohm-cm and all epitaxial layers were grown on 100 mm Si (111) wafers in a custom-built, cold wall, rotating disc MOCVD reactor at nominally 1030 °C. The growth process used in this experiment is based on the growth of crack-free GaN epi layers on Si, which has been detailed previously<sup>7</sup>.

The first set of samples, designated as Experiment A, contained  $\sim 1000$  Å of AlN deposited at 1030 °C in 15 minutes. The sample was then held at 1030 °C for an additional 165 minutes under an over pressure of ammonia. This was done to expose the AlN/Si wafer to the MOCVD environment for the typical growth time of the HEMT process.

This sample was characterized by mapping the sheet resistance across the wafer. Then, half the wafer was covered with photo-resist and the exposed AlN film was etched completely using an inductively coupled plasma (ICP) source in chlorine and boron-trichloride chemistry. Etching conditions were optimized to minimize any over-etch into the silicon substrate itself. Secondary ion mass spectroscopy (SIMS) was carried out on the etched half to analyze the impurities in the substrate that may be present due to the interaction of the substrate with the MOCVD environment during growth of III-N layers. Finally, spreading resistance profiling (SRP) measurements were carried out on the un-etched half of the wafer, in order to determine the carrier concentration in the silicon as a function of depth below the AlN/Si interface.

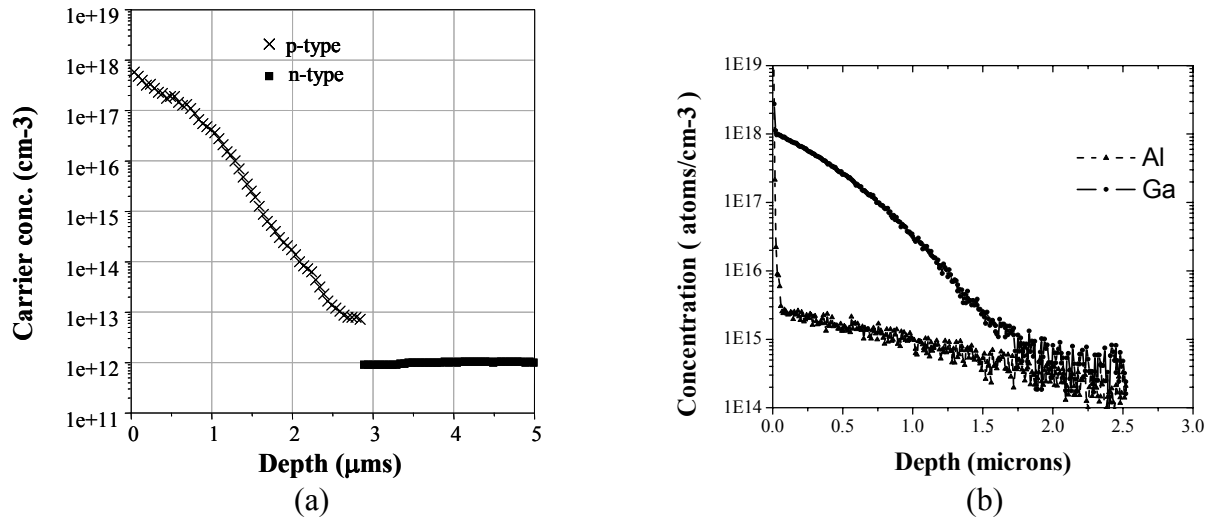
The second set of samples (Experiment B) consisted of AlGaIn/GaN HEMTs grown using an optimized transition layer scheme that resulted in crack free GaN buffer layers. Additional details of the growth and of the fabrication are reported elsewhere<sup>9,10</sup>. The device layer consisted of  $\sim 275$  Å of 20% UID AlGaIn. The fabricated devices, which had a nominal gate length of  $0.7\mu\text{m}$ , were tested in several ways. Large signal power sweeps were obtained at 2.14 GHz with the drain  $V_{ds}$  at 28 V. The gate was biased such that quiescent current was 25% of maximum channel current. Small signal characterization was performed on a through structure to estimate microwave transmission loss to the substrate. Small signal characterization was also carried out on fully fabricated transistors to determine the cut off frequency ( $f_T$ ) and maximum frequency of oscillation ( $f_{max}$ ).

## Results and Discussion

The sheet resistance of a bare substrate prior to growth was greater than the upper measurement limit of  $\sim 10^5$  ohms/square. However, the mean sheet resistance of an Experiment A sample was 598 ohms/square. This indicated a change in the conductivity of the substrate, as the AlN is assumed to be an insulator. SRP proved to be a very effective method to investigate the conductivity and carrier type in the Si substrate at the AlN/Si interface. In the SRP technique, two closely spaced probes are stepped down the face of a shallow bevel that has been prepared on the sample. The resistance is measured and the carrier concentration is calculated. Hot point probe capability is usually built in to the apparatus allows for determination of the carrier type, and the shallow bevel allows for very high depth resolution. The carrier concentration as determined by SRP of an Experiment A sample is shown in Fig. 1(a).

The SRP measurement performed on the Si substrate reveals p-type conductivity with a maximum carrier concentration of  $\sim 8 \times 10^{17}$  close to the AlN/Si interface. The carrier concentration decreases steadily and remains p-type to a depth of  $\sim 2.8 \mu\text{m}$  into the Si substrate. At this depth, the carrier type reverts to n-type at a level commensurate with the known resistivity of the starting substrate. Thus, there is a localized reduction in the substrate resistivity, while the bulk of the substrate below the p-type region appears relatively unchanged.

Analysis of the Si substrate by SIMS (Fig. 1(b)) shows the presence of Al and Ga elements, both of which will lead to p-type conductivity in Si. The maximum Ga concentration is  $\sim 1 \times 10^{18} \text{ cm}^{-3}$  and that of Al is  $5 \times 10^{16} \text{ cm}^{-3}$  in the Si substrate. The maximum Ga concentration and its profile are similar to the maximum carrier concentration and its profile determined by SRP, indicating that Ga adsorption onto the Si surface prior to nucleation, and subsequent diffusion into the silicon during growth is the dominant factor in reducing the resistivity of the silicon substrate during growth. It is also clear that this p-type parasitic channel is present in the Si and validates the assumption that the AlN is an insulator, at least to the first order. Since Ga precursor is not intentionally introduced during heat-up or nucleation, we suspect that residual by-products in the MOCVD reactor are the primary source of Ga found in the substrate. However, the source of Al in the substrate could either be from residual Al in the MOCVD reactor or from the Al precursor introduced in the initial stages of the nucleation. It is possible that Al adatoms adsorb on the Si surface and do not incorporate fully into the AlN lattice. This Al could continue to diffuse into the substrate during growth. It should also be noted that the levels of Al are close to the lower detection limits of SIMS ( $\sim 1\text{-}2 \times 10^{15} \text{ atoms}\cdot\text{cm}^{-3}$ ). In any case, the presence of a conductive layer at the AlN/Si interface can lead to parasitic losses of RF energy and degrade performance of fabricated devices. Process improvements were implemented to minimize the formation of this parasitic p-type conductive layer.

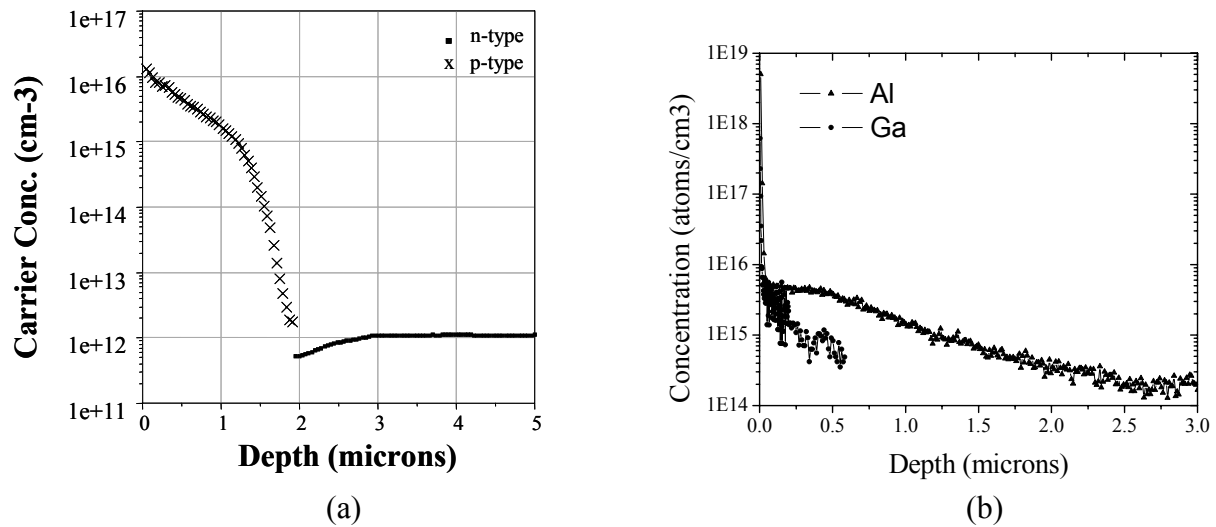


**Figure 1(a).** Carrier concentration profile and carrier type in the Si substrate vs. depth by SRP. **(b)** Ga and Al concentration in the Si substrate vs. depth by SIMS.

Since residual reaction by-products in the reactor were thought to be the main source of the impurities in the silicon substrate, process changes were implemented that minimized deposition of by-products on chamber components. The total gas flow into the reactor, which included critical purge flows intended to keep chamber walls and components clean, was increased by nominally 60%. The increased overall flow, in addition to flushing reaction by-products more efficiently, may also help suppress recirculation. This higher total-flow process was then re-optimized for uniform film deposition of the various III-N layers forming the AlGa<sub>0.3</sub>N/GaN HEMT structures.

Using this revised growth process, termed the “high-flow” process, another experiment A sample was grown and analyzed. The mean value of the sheet resistance for this wafer was

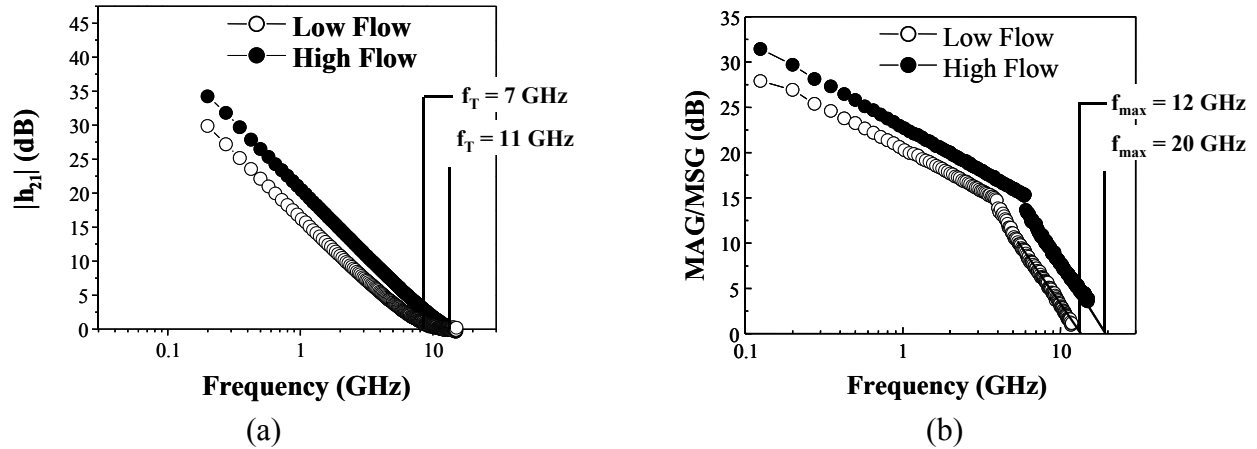
10,508 ohms/square, which is more than an order of magnitude higher than with the initial process. The SRP and SIMS data for this sample are shown in Figure 2. The SRP data of Figure 2(a) shows that the p-type carrier concentration in the Si substrate at the AlN/Si interface surface has been reduced by nearly two orders of magnitude, to a level of  $\sim 1 \times 10^{16} \text{ cm}^{-3}$ . The SIMS data in Figure 2(b) shows that the Ga concentration in the Si substrate has been decreased dramatically. The Ga in the Si substrate is below  $10^{16} \text{ atoms/cm}^3$  and is essentially at the detection limit of SIMS. The Al profile in the Si substrate, on the other hand, appears relatively unchanged when compared with the initial sample. This supports the hypothesis that the Al found in the Si substrate may be an artifact of the nucleation process and not the residual by-products in the MOCVD reactor. Notwithstanding the Al analysis by SIMS, the sheet resistance, SRP, and SIMS data all indicate that implementing the high-flow process change has substantially reduced the p-type parasitic conductive layer in the Si substrate.



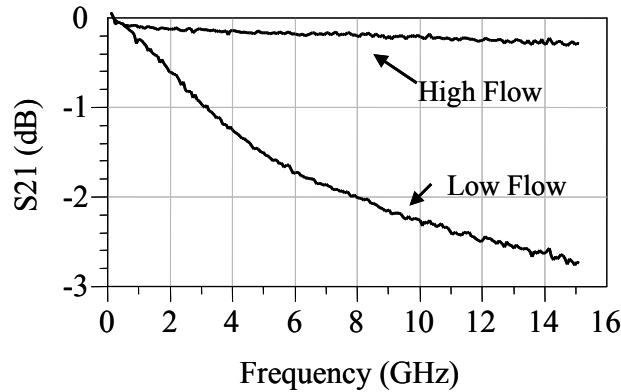
**Figure 2**(a) Carrier concentration profile and carrier type in the Si substrate vs. depth by SRP. (b) Ga and Al concentration in the Si substrate as a function of depth by SIMS.

The RF performance of devices is expected to be impacted by the change in conductivity of the Si at the Si/III-N interface. To investigate this effect, HEMTs were fabricated using both the low and the high flow processes. The HEMT structure consisted of  $\sim 275 \text{ \AA}$  of unintentionally doped  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$ . The fabricated field effect transistors (FETs) had 2 mm gate periphery ( $200 \text{ \mu m}$  gate width x 10 fingers) devices, with a  $\sim 0.7 \text{ \mu m}$  gate length. The source-gate and drain-gate distances were  $1 \text{ \mu m}$  and  $3 \text{ \mu m}$  respectively. The cut off frequency ( $f_T$ ) and the maximum frequency ( $f_{\text{max}}$ ) of the devices are shown in Figure 3. The  $f_T$ , shown in Figure 3(a), increased from 7GHz to 11GHz while the  $f_{\text{max}}$ , shown in Figure 3(b), increased from 12 GHz to 20 GHz when the process was changed from low flow to high flow. Additionally, a 50-ohm coplanar transmission line on the wafer was used to characterize microwave transmission loss as a function of frequency. This structure was fabricated in a region of the wafer where the two-dimensional electron gas (2DEG) had been eliminated.  $S_{21}$  measurement as a function of frequency shows dramatically reduced loss to the substrate for the growth process with higher flow. Alternately, in the case of the lower flow process, losses are experienced due to capacitive coupling of the RF energy with the parasitic p-type layer at the AlN/Si interface. The reduction

in microwave transmission loss will enhance performance of AlGaN/GaN HEMTs at higher frequencies.



**Figure 3** (a) and (b).  $f_T$  and  $f_{max}$  measurements on 20% AlGaN/GaN HEMT wafers grown using the low and the high flow process.



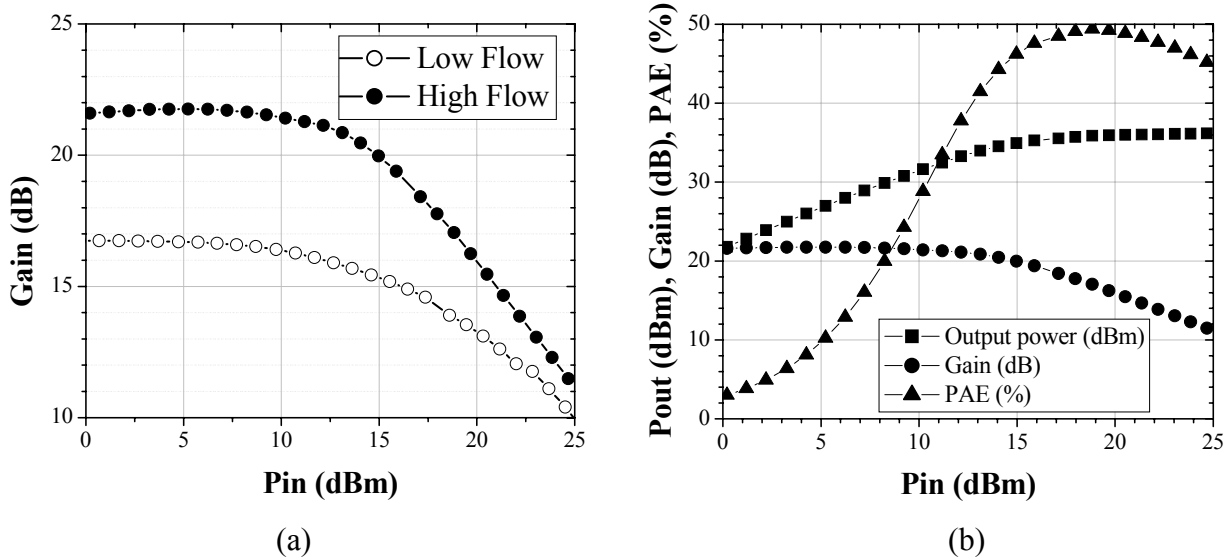
**Figure 4.** Small signal  $S_{21}$  measurements on a through structure for both the low and the high flow processes.

Large signal power measurements were carried out on 2 mm gate periphery devices with  $V_{ds} = 28$  V and quiescent current of 25% of  $I_{dmax}$  at a frequency of 2.14 GHz. The wafers grown using the high-flow process showed a  $\sim 4$  dB improvement in gain, as shown in Figure 5(a). The power sweep of a device grown using the high flow growth process tested at  $V_{ds} = 28$  V is shown in Figure 5(b). This shows a saturated power output of 2 W/mm and maximum power added efficiency (PAE) of  $\sim 50\%$  with a small signal gain of 21 dB.

## Conclusions

The MOCVD growth process used to deposit III-N layers on Si can leave by-products containing Ga and Al in the MOCVD reactor. These by-products can potentially redeposit onto the Si substrate during growth and reduce the resistivity of the Si at the Si/III-N interface, which in turn caused degradation in small and large signal RF parameters. An improved epi process has been implemented to minimize the incorporation of the by-products in the Si during the initial stages of growth, thereby minimizing the formation of a p-type parasitic channel at the surface of the Si

substrate. This has resulted in improved device performance as evidenced by an increase in  $f_T$  from 7 to 11 GHz,  $f_{max}$  from 12 to 20 GHz and small signal gain from ~17 dB to ~21 dB.



**Figure 5(a).** Large signal gain sweep of Experiment B devices grown using low flow (open circles) and high flow (filled circles) MOCVD process. (b) A power measurement of a packaged 2 mm cell grown using high flow growth process, with  $V_{ds} = 28$  V showing a small signal gain of 21 dB, saturated power density of 2W/mm and PAE maximum of  $\approx 50\%$ .

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