Large-Area, Device Quality GaN on Si Using a Novel Transition Layer Scheme

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ABSTRACT

The emergence of III-nitride technology and fabrication of high quality GaN based devices is possible due to the advances in the heteroepitaxial growth of III-N thin-films on lattice-mismatched substrates. Typically, the substrate of choice is either SiC or sapphire. We have adopted 100mm Si as our substrate of choice; uniform substrates of high quality are inexpensive and plentiful due to decades of use in the microelectronics industry. Growth of device quality GaN on Si is challenged by the ~17% lattice mismatch and an additional thermal expansion coefficient (TEC) mismatch of ~56%. In order to accommodate this strain and TEC mismatch between Si and GaN, a novel transition layer was designed, grown and successfully optimized, obviating the need for either a PENDEO® based overgrowth process or a SiC interlayer-based process. This growth technique (SIGANTIC®) does not require any wafer conditioning prior to growth and thus reduces the process complexity and maintains the cost effectiveness of the GaN on Si strategy. We will report on this manufacturable 100mm MOCVD heteroepitaxial process that consistently produces device quality AlGaN/GaN heterostructures with two dimensional electron gas (2DEG) mobilities typically around 1400 cm^2/Vs at room temperature. Structural and electrical properties as determined by optical reflectance, atomic force microscopy, capacitance-voltage and van der Pauw Hall measurements, which are measured across the 100mm wafer, will be presented. Device results will be mentioned to show continuous wave (CW) RF operation at 2 GHz with competitive power output, gain and power added efficiency (PAE).

INTRODUCTION

Growth of high quality GaN on Si (111) can be achieved only by addressing the significant levels of lattice misfit (~17%) and TEC (~ 56%) mismatch. A schematic of the lattice misfit is shown in Figure 1 (a). It is clear, that the lattice misfit effects will dominate the Si/III-N interface, where a high density of misfit dislocations are expected to form during growth. For example, the choice of using AlN as a nucleation layer on Si (111) results in the formation of an estimated maximum of ~3×10^{12} cm^{-2} misfit dislocations near the Si/AlN interface. It will be shown that despite the high density of defects that are expected to be present in the AlN layer, these do not appear to impact the 2DEG properties of subsequently deposited AlGaN/GaN device layers.

The TEC mismatch between GaN and Si ($\alpha_{GaN\parallel} = 5.59 \times 10^{-6}$/K, for T >= 300K, $\alpha_{Si} = 3.59 \times 10^{-6}$/K @ 300K[1]) poses a completely different challenge and is shown in figure 1 (b). The TEC mismatch results in stress (σ) within the film, which can be calculated from equation 1 as,

$$\sigma = \Delta\alpha\Delta T E_f \qquad (1)$$

Where Δα is the TEC mismatch between GaN and Si, ΔT is the difference between the growth temperature of the film and room temperature, and E_f is the Young's modulus of the film. The magnitude of this stress is fixed for a given combination of substrate, film and growth temperature. This stress manifests itself during cooldown, and must be adequately accommodated by the film-substrate combination to result in crack free GaN films.

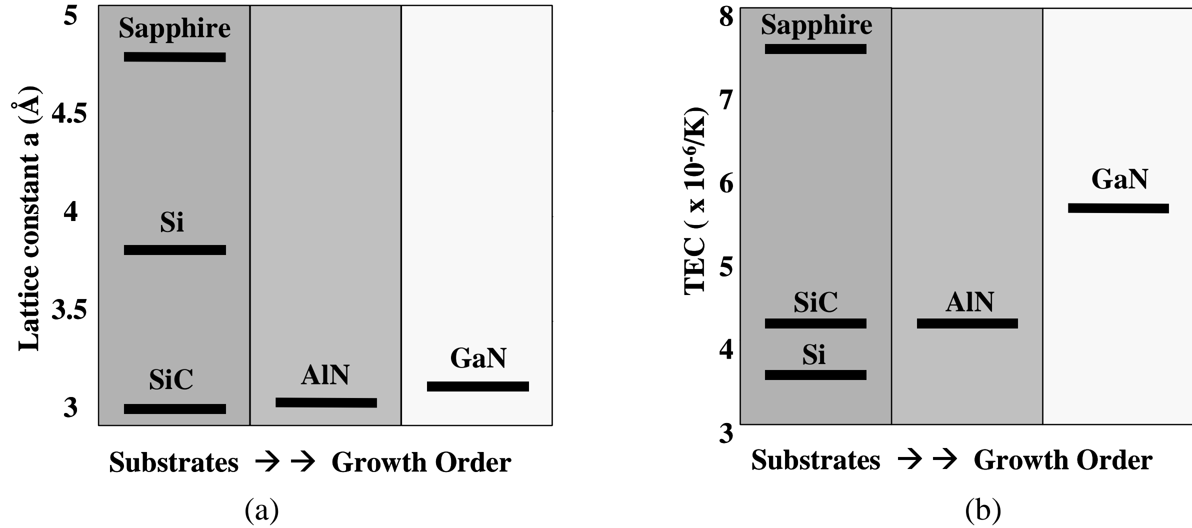


Figure 1. Schematic of the epitaxial challenges in growing crack free GaN on Si (111) including (a) the lattice misfit and (b) the TEC mismatch. In both figures, the typical substrates are grouped to the left, AlN in the middle and GaN to the right in order to preserve a typical growth sequence.

Several groups have made efforts to manage this high level of lattice and thermal mismatch [2, 3, 4, 5, 6,] with varying degrees of success. At Nitronex, a novel growth process, SIGANTIC®, has been developed that results in the growth of crack-free GaN, which has been used to fabricate GaN-based devices in both microelectronic and optoelectronic areas [7, 8, 9, 10]. Previously at Nitronex, this approach was successfully used to develop InGaN/GaN MQW LEDs emitting at a nominal wavelength of 450 nm[11]. This paper will focus on the growth and characterization of AlGaN/GaN based high electron mobility transistor (HEMT) structures for high-power and high frequency applications. Material and electron transport characteristics will be reported along with a brief mention of the device characteristics.

EXPERIMENTAL

The AlGaN/GaN heterostructures were grown on 100 mm Si (111) wafers in a custom-built, cold wall, rotating disc MOCVD reactor at nominally 1000 ºC. The device layers consisted of ~250 Å of 25% UID AlGaN capped with 50 Å of UID GaN. The reactor design enables control of temperature and flow across multiple zones allowing for development of uniform processes. Trimethylgallium (TMG) and trimethylaluminium (TMA) precursors were carried by Pd-diffused hydrogen and ammonia (NH_3) was used as the N precursor. The material and electron transport characteristics of the wafers were characterized using white light reflectance thickness mapping, atomic force microscopy (AFM), scanning transmission electron microscopy (STEM), Hg-probe capacitance-voltage (C-V) profiling, van der Pauw Hall measurements and four-point probe sheet resistance mapping. The two dimensional electron gas (2DEG) channel characterization by van der Pauw Hall effect measurements were made on 7mm x 7mm samples,

which were diced from as grown wafers. Channel sheet resistance was also measured on 100 µm x 100 µm van der Pauw mesa structures, which are fabricated adjacent to and concurrently with production die. A Ti/Al/Ni/Au annealed ohmic contact scheme was used for both measurements.

RESULTS AND DISCUSSION

The highlights of the HEMT growth process are as follows: (a) heat up the wafers in an environment that prevents nitridation of the Si (111) wafers, (b) AlN is nucleated on Si (111) which also acts as a barrier against undesirable Ga-Si interaction, (c) the (Al, Ga) N transition layer is deposited using optimized process conditions (d) unintentionally doped (UID) GaN buffer is deposited and (e) $Al_xGa_{1-x}N$ device layers are deposited. Using this single step approach, crack free GaN with excellent material characteristics and uniformity are routinely deposited on 100 mm Si (111) substrates. Wafers also exhibit negligible bow as is evidenced by radii of curvature in excess of 30 m.

The growth conditions were optimized to result in a high level of thickness uniformity, as measured by white light reflectance shown in Figure 2. The total film thickness was 2020 nm with a total thickness variation of 5.1% (5 mm edge exclusion). AFM performed on 5 µm x 5 µm areas revealed a smooth surface with an RMS roughness in the 5-10 Å range. A similar scan of a 1 µm x 1 µm shows roughness in the 2.5-5 Å range as shown in Figure 3a. A defect density on the order of ~ 2 x 10^9 cm^{-2} was estimated from the AFM image. The sharpness of the AlGaN/GaN heterointerface is also confirmed by scanning transmission electron microscopy (STEM) as shown in Figure 3b.

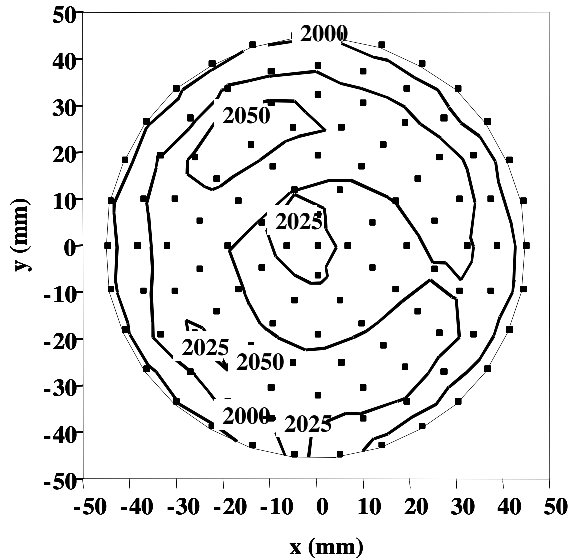


Figure 2. White light reflectance thickness map of an AlGaN/GaN HEMT wafer grown on a 100 mm Si (111) substrate. The average epi thickness was 2020 nm with a total thickness variation of 5.1%.

Transport characteristics of the channel have been evaluated by several methods. Room temperature (RT) van der Pauw Hall measurements are periodically performed and routinely result in mobilities in the 1300-1500 cm^2/V-s range and sheet charge densities in the 7.5-8.5 x 10^{12} cm^{-2} range. Non-destructive sheet resistance measurements are also performed on van der

Pauw test mesas that are distributed across fully fabricated wafers. Sheet resistances in the range of 450-550 ohms/square are typically observed and are in good agreement with the sheet resistances obtained from Hall measurements. Figure 4a shows a typical 100 mm wafer map of sheet resistance measured across a fully fabricated wafer; the range of values is distributed between 450-550 ohms/square, with the majority of the data in the 450–470 ohms/square range. Figure 4b tabulates RT mobility, sheet charge, and sheet resistance data obtained from destructive Hall measurement at five points from the center toward the edge of the 100 mm wafer. The high values of mobility validate the quality of the epitaxial film and the interface smoothness, resulting in a high quality channel obtained uniformly across the 100 mm wafer.

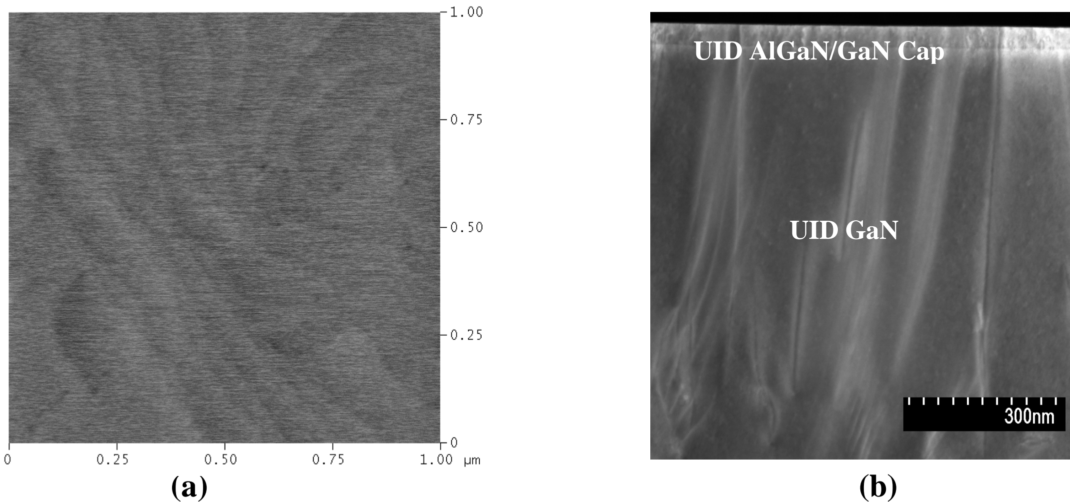
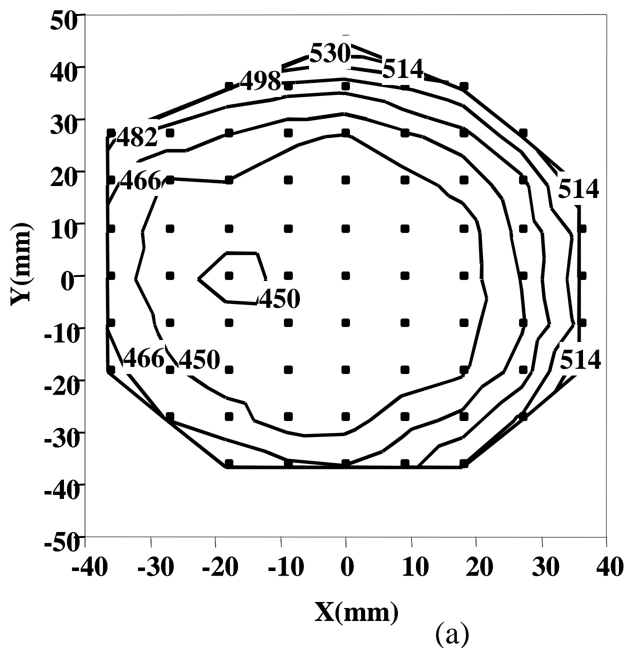


Figure 3. (a) 1 μm x 1 μm AFM image of the AlGaN/GaN HEMT wafer with an RMS roughness of 2.5 Å (b) STEM image of the AlGaN/GaN heterostructure.



(a)

Position from center (mm)	Mobility (cm^2/V s)	Sheet Charge (x $10^{12}cm^{-2}$)	Sheet Resistance (ohms/square)	AlN% [12, 13]
8	1553	7.7	520	24.6
15	1581	8.1	487	25.7
22	1572	8.7	455	26.8
30	1541	8.4	481	27.3
38	1436	7.8	560	27.3

(b)

Figure 4. (a) Sheet resistance map (ohms/square) taken from van der Pauw mesas over a fully fabricated 100 mm wafer, (b) Mobility (cm^2/V s), sheet charge (cm^{-2}), and sheet resistance (ohms/square) derived from destructive Hall measurement at five points across an as-grown epi wafer.

Characteristics of the AlGaN/GaN HEMT channel are also routinely assessed by Hg-probe C-V measurements. Doping vs. depth profiles were calculated from raw C-V data using commercial software. The C-V data for a typical AlGaN/GaN HEMT is shown in Figure 5, which exhibits a pinch off voltage of ~4.4 V. The plot of doping vs. depth exhibits a maximum electron concentration of ~1 x 10^{20} cm^{-3} at a depth of ~200Å from the surface. The high concentration of electronic charge indicated by the steep doping profile is another indication of a high degree of channel confinement. The absence of a complete peak (i.e., no "roll over") in the doping vs. depth profile is apparently a result of zero-volt surface depletion of the mercury contact.

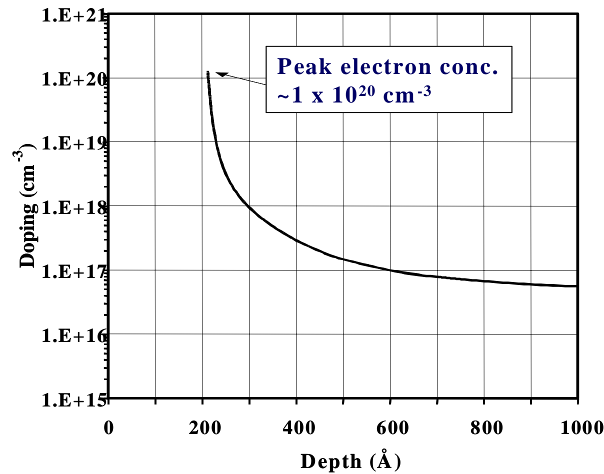


Figure 5. Doping vs. depth profile derived from C-V measurements.

The absence of cracks and excellent electrical and material characteristics imply that the lattice misfit and TEC mismatch have been adequately addressed by the transition layer scheme described above. The transition layer addresses the two challenges necessary for the successful growth of GaN on Si: It manages both the lattice and thermal mismatch between the two materials. A simplified explanation would be to speculate that the AlN/Si interface absorbs most of the lattice mismatch while the (Al,Ga)N transition layer is successful in absorbing the stresses that arise due to the TEC mismatch. Initial investigations have revealed that in order to prevent cracking of the AlGaN/GaN HEMT wafer, it is important to optimize the thickness and the nature of the composition profile of the transition layer. The growth conditions of the transition layer have also been determined to be significant; this suggests a role played by the nature and density of defects and the resultant material properties of the transition layer. Studies are underway to gain further insight into the effectiveness of the transition layer; it is hoped that this will lead to a physical model to help explain the stress states in GaN on Si.

The AlGaN/GaN HEMT wafers grown using the SIGANTIC® process were fabricated into power transistors. The transistor was fabricated with Ti/Al/Ni/Au source and drain ohmic contacts, a Ni/Au Schottky gate with 1 µm gate length, and a SiN_x passivant deposited by plasma enhanced chemical vapor deposition. The median values for I_{dss}, I_{dmax} and maximum g_m for the 25% UID AlGaN/GaN HEMT over a recent batch of 19 wafers were 576 mA/mm, 862 mA/mm and 183 mS/mm respectively. (The term I_{dmax} refers to the maximum drain current and is measured at a fixed forward gate voltage of 3.5 V with the drain biased at 7 V). The continuous wave (CW) RF characteristics of 300 µm devices at 2 GHz were measured where the test conditions were V_{ds} = 30 V and the gate was biased for optimized class A operation. Under

these conditions, a power density of 3.3 W/mm of saturated RF power was achieved. The linear gain was 16 dBm with a maximum power added efficiency (PAE) of 30%. We also measured devices with 18 mm total gate width at 2.14 GHz, CW operation with the device in class AB mode and the drain at 28 V; the saturated power, linear gain and PAE were 27 W, 14 dB and 45% respectively [9] for this large device. These numbers are among the highest reported for AlGaN/GaN power devices.

CONCLUSIONS

High quality AlGaN/GaN HEMT structures grown on 100 mm Si (111) substrates have been uniformly deposited using an (Al,Ga)N based transition layer scheme. The crack free wafers exhibit exceptional transport characteristics, which imply the presence of a high quality 2DEG with high channel mobilities (1300-1500 cm^2/Vs) and channel sheet charge densities (7.5-8.5 x 10^{12} cm^{-2}). Fabrication of power transistors on these wafers produced excellent DC and RF characteristics (CW) that are among the highest reported for AlGaN/GaN HEMTs.

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REFERENCES

[1] P. R. Hageman, S. Haffouz, A. Grzegorczk, V. Kirilyuk, and P. K. Larsen, Mat. Res. Soc. Symp. Proc. **693**, 105 (2002).
[2] Min-Ho Kim, Young-Gu Do, Hyon Chol Kang, Do Young Noh and Seong-Ju Park, Appl. Phys. Lett. **79**, 2713 (2001).
[3] Eric Feltin, B. Beaumont, M. Laugt, P. de Mierry, P. Vennéguès, H. Lahrechè, M. Leroux, and P. Gibart, App. Phys. Lett. **79**, 3230 (2001).
[4] A. Dadgar, M. Poschenrieder, J. Bläsing, K. Fehse, A. Diez, and A. Krost, Appl. Phys. Lett. **80**, 3670 (2002)
[5] Yankun Fu, and Daniel A. Gulino, J. Vac. Sci. Technol. A **18**(3), 965 (2000).
[6] Eduardo M. Chumbes, A. T. Schremer, Joseph A. Smart, Y. Wang, Noel C. MacDonald, D. Hogue, James J. Komiak, Stephen J. Lichwalla, Robert E. Leoni, James R. Shealy, IEEE Transactions of Electron Devices, **48**, No. 3, March 2001, 420 (2001).
[7] Walter Nagy, Jeff Brown, Ricardo Borges, and Sameer Singhal, to be published.
[8] A. Vescan, J. D. Brown, J. W. Johnson, R. Therrien, T. Gehrke, P. Rajagopal, J. C. Roberts, S. Singhal, W. Nagy, R. Borges, E. Piner, and K. Linthicum, Phys. Stat. Sol. (c) (2002) to be published.
[9] S. Singhal, J.D. Brown, R. Borges, E. Piner, W. Nagy, A. Vescan, GAAS 2002 Conference Proceedings, Milan, Italy. Sept. 23-27 (2002).
[10] J. D. Brown, Ric Borges, Edwin Piner, Andrei Vescan, Sameer Singhal, Robert Therrien, Solid State Electronics, **46** 1535 (2002).
[11] Warren Weeks, Ricardo Borges, Compound Semiconductor, **7**, 63 (2001).
[12] L. S. Yu, D. Qiao, S. S. Lau, and J. M. Redwing, App. Phys. Lett., **75**, 1419 (1999).
[13] H. Jiang, G. Y. Zhao, H. Ishikawa, T. Egawa, T. Jimbo, M. Umeno, J. App. Phys., **89**, 1046 (2001).