12 W/mm AlGaN–GaN HFETs on Silicon Substrates

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***Abstract*—$Al_{0.26}Ga_{0.74}N$–GaN heterojunction field-effect transistors were grown by metal–organic chemical vapor deposition on high-resistivity 100-mm Si (111) substrates. Van der Pauw sheet resistance of the two-dimensional electron gas was 300 Ω/square with a standard deviation of 10 Ω/square. Maximum drain current density of ~1 A/mm was achieved with a three-terminal breakdown voltage of ~200 V. The cutoff frequency and maximum frequency of oscillation were 18 and 31 GHz, respectively, for 0.7-μm gate-length devices. When biased at 50 V, a 2.14-GHz continuous wave power density of 12 W/mm was achieved with associated large-signal gain of 15.3 dB and a power-added efficiency of 52.7%. This is the highest power density ever reported from a GaN-based device grown on a silicon substrate, and is competitive with the best results obtained from conventional device designs on any substrate.**

***Index Terms*—GaN, heterojunction field-effect transistor (HFET), high electron mobility transistor (HEMT), power density, silicon.**

I. Introduction

INCREASING performance requirements (e.g., power density, bandwidth, operation temperature, voltage rating) are fueling the demand for wide bandgap electronic device development in areas such as satellite and radar communication systems, wireless basestations, high temperature electronics, and high power solid-state switching. Gallium nitride (GaN) and its alloys represent one of the most attractive material systems for such applications. AlGaN–GaN heterostructure field-effect transistors (HFETs) have been widely investigated over a broad frequency range from S-band to V-band, with nearly all structures heteroepitaxially grown on sapphire (Al_2O_3) or silicon carbide (SiC) substrates. For sapphire, the current state-of-the-art power density of 12 W/mm at 4 GHz was recently reported by Chini *et al.* [1] using a field-plated structure. Optimization of similar field-plated HFETs grown on SiC substrates led to 32.2 W/mm at 4 GHz by Wu *et al.* [2]. Despite these excellent results, sapphire substrates are hindered by poor thermal conductivity [3] and SiC substrates suffer from high cost, intrinsic material defects, and lack of widespread commercial availability for diameters >75 mm. AlGaN–GaN HFETs on high-quality, large-area, low-cost Si substrates are viewed as an attractive alternative to some of the limitations presented by sapphire and SiC. Performance of GaN-based devices on silicon, however, has lagged behind that of similar devices on sapphire and SiC, mainly due to difficulties associated with crystal growth. Typical HFETs on Si have achieved power densities of 1–3 W/mm at S-band [4]–[10]. Behtash *et al.* recently reported molecular beam epitaxy HFETs on Si with 2-GHz continuous wave (CW) power density of 6.6 W/mm [11]. In this letter, we present $Al_{0.26}Ga_{0.74}N$–GaN HFETs grown on high-resistivity Si (111) substrates that achieve a record-setting 12 W/mm saturated output power density. By simultaneously optimizing current-handling capability and breakdown voltage through epi structure and device processing details, these devices achieved ~1 A/mm drain current density and breakdown voltage of ~200 V. Details of epi characteristics and 100-mm wafer uniformity, as well as the resultant dc and RF device performance will be given.

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II. Material Growth and Device Fabrication

All layers in this study were grown by metal–organic chemical vapor deposition (MOCVD) using conventional precursors in a cold-wall, rotating disc reactor designed from flow dynamic simulations. The growth process was nucleated with AlN to avoid unwanted Ga–Si interactions. The epitaxial stack then consisted of a proprietary AlGaN transition layer [12] to accommodate thermal and lattice mismatch and a ~800-nm unintentionally doped GaN buffer layer. Typical device structures consisted of 16–20 nm total thickness of (Al,Ga)N barrier and capping layers. For this letter, the Al content of the barrier was 26%. The nominal growth temperature for the GaN buffer and all device layers was 1030 °C.

Transistor fabrication began with Ti–Al–Ni–Au ohmic metallization and rapid thermal annealing in flowing N_2 at ~825 °C. Contact resistance, specific contact resistivity, and specific on-resistance were 0.45 Ωmm, 5×10^{-6} Ωcm^2, and 2.2 Ωmm, respectively. Immediately following ohmic anneal, the wafers were passivated with 900 Å of plasma-enhanced chemical vapor-deposited SiN_x. Interdevice isolation was accomplished by multiple energy N^+ implantation to produce significant lattice damage throughout the thickness of the GaN buffer layer. The ion implantation step is attractive not only to maintain a planar geometry in the fabricated device, but has also been shown to reduce leakage paths that can exist in passivated, mesa-isolated HFETs [14], [15]. Schottky contacts were formed by selectively removing the SiN_x passivation layer in a fluorine-based dry etch chemistry and subsequent deposition of 0.7 μm dielectrically defined Ni–Au gates. Large periphery devices were airbridged for source interconnection to a thickness of ~3 μm using standard Au electroplating techniques.

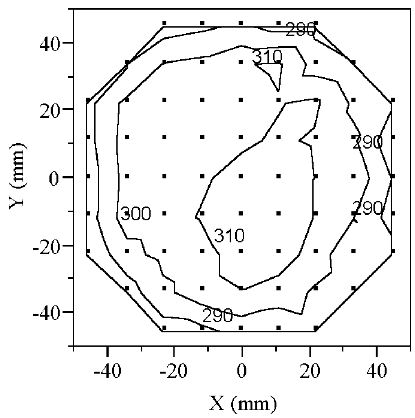

Fig. 1. Van der Pauw sheet resistance uniformity contours for $Al_{0.26}Ga_{0.74}N$–GaN HFET wafer. The mean and standard deviation of R_{sh} across the 100-mm diameter are 300 $\Omega/$square and 10 $\Omega/$square, respectively.

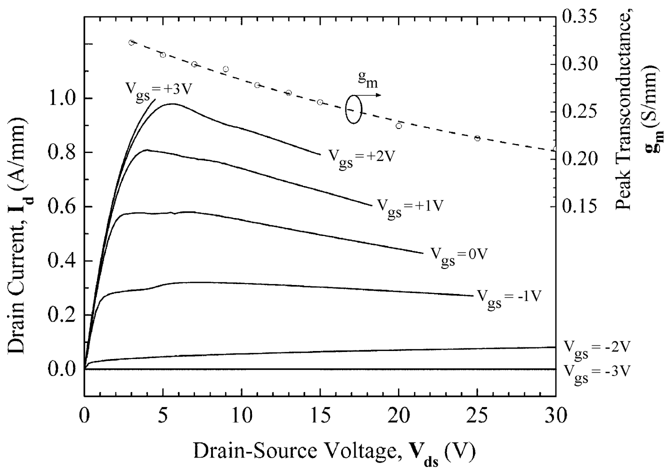

Fig. 2. Output characteristics of 100-μm gate width AlGaN–GaN HFET illustrating 1 A/mm drain current density. Also shown is extrinsic transconductance as a function of V_{ds} with peak g_m of 325 mS/mm. Transconductance of $>$200 mS/mm is maintained beyond $V_{ds} = 30$ V.

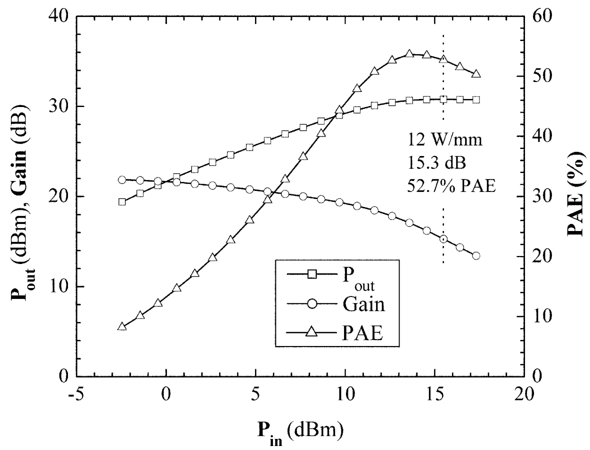

Fig. 3. Continuous-wave 2.14 GHz power sweep of 2 $\times$ 50 μm $\times$ 0.7 μm $Al_{0.26}Ga_{0.74}N$–GaN HFET. Bias conditions were $V_{ds} = 50$ V and $V_{gs} = -1.1$ V ($I_{dq} = 0.21$ A/mm).

III. Results and Discussion

A sheet resistance (R_{sh}) uniformity map obtained from van der Pauw cross bridge measurements of a passivated 100-mm $Al_{0.26}Ga_{0.74}N$–GaN HFET wafer is given in Fig. 1, illustrating a mean R_{sh} of 300 $\Omega/$square. This corresponds to an excellent 2DEG sheet charge $\times$ mobility product of 2.1×10^{16} $(Vs)^{-1}$. The standard deviation of R_{sh} across the 100-mm diameter (with 5-mm edge exclusion) was 10 $\Omega/$square with full-scale range ($R_{sh,max}$–$R_{sh,min}$) of 38 $\Omega/$square.

Fig. 2 shows typical output characteristics of a 2 $\times$ 50 μm $\times$ 0.7 μm HFET with drain current density of $\sim$1 A/mm and excellent pinchoff characteristics. Process control monitor (PCM) single-finger 100-μm gate width transistors were probed on each of the 69 reticles of the 100-mm wafer, and yielded a mean maximum drain current density of 1040 $\pm$ 40 mA/mm (defined at a forward gate current density of 1 mA/mm) with no excluded die. Fig. 2 also gives the drain bias (V_{ds}) dependence of the maximum extrinsic transconductance (g_m) for V_{ds} up to 30 V. The peak extrinsic g_m reached 325 mS/mm at low V_{ds} and remained greater than 200 mS/mm beyond V_{ds} of 30 V. From the measured source resistance of 0.86 Ωmm, a maximum intrinsic g_m of 450 mS/mm was estimated. The gate-source bias corresponding to the transconductance peak shifted from -1.4 V at $V_{ds} = 5$ V to -1 V at $V_{ds} = 30$V.

Three-terminal destructive breakdown voltage for small periphery devices was 60–70 V per micron of gate-drain spacing, yielding $\sim$200 V for the geometry used in this study. Die yield for breakdown voltage was $\sim$90%, with all excluded (failed) die originating from the wafer perimeter, likely due to processing irregularities. Average drain leakage current density measured on PCM 2 $\times$ 200 μm gate width devices was $\sim$0.3 mA/mm at $V_{ds} = 150$ V and $V_{gs} = -8$ V. The leakage/breakdown behavior was dominated by the gate-drain diode at all voltages.

Scattering parameters were measured with an Agilent 8510C Vector Network Analyzer calibrated to 30 GHz. Wafers were thinned to $\sim$ 150 μm and backmetallized with 0.5 μm Au prior to small- and large-signal RF data collection. At $V_{ds} = 15$ V and quiescent current (I_{dq}) of 25% $I_{D,max}$, measured values of cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were 18 and 31 GHz, respectively. The $f_T \times$gate length product of 12.6 GHz$\cdot\mu$m is one of the highest values ever reported for AlGaN–GaN HFETs on Si [4], [7]–[11].

All large-signal measurements were performed on-wafer at 2.14 GHz under CW conditions using Focus Microwaves tuners. Data were collected at 25 °C from 2 $\times$ 50 μm $\times$ 0.7 μm HFETs on thinned, backmetallized wafers. No through-wafer vias were present. Devices were biased at $V_{ds} = 50$ V and $V_{gs} = -1.1$ V and were matched for gain and power on the input and output, respectively. Tuning was performed at an input power level of 13 dBm. At the optimized tuner states, the source and load reflection coefficients at the DUT were $\Gamma_{source} = 0.77e^{j18^\circ}$ and $\Gamma_{load} = 0.85e^{j1^\circ}$. The system integrity was verified to a net loss of 0.3 dB on a 50 Ω through. A 50 V power sweep is shown in Fig. 3, illustrating 30.8 dBm saturated output power with associated large-signal gain of 15.3 dB and power-added efficiency (PAE) of 52.7%. This corresponds to a power density of 12 W/mm and, to the best of the authors' knowledge, represents the highest power density ever reported for a GaN-based device grown on a silicon substrate. Peak PAE and drain efficiency reached 53.7% and 54.8%, respectively. However, the maximum impedance of $\sim$ 600 Ω available from the output tuner resulted in a current-limited load line for these small periphery devices. Drain efficiency values of $\sim$70% were obtained in class AB operation on larger devices and at lower V_{ds}, where proper matching was obtainable with a reduced load impedance. A systematic study of device scaling and power versus efficiency tuning optimization will be presented elsewhere.

The large-signal results presented in this letter are attributable to optimization of both MOCVD growth details and the HFET device processing sequence. Growth conditions have been optimized to reduce extrinsic point defect concentration and parasitic contributions from the substrate. Control of point defects in the GaN buffer has been shown to reduce RF dispersion and increase efficiency. Reduction of the p-type parasitic channel at the Si surface decreases microwave loss to the substrate, improving both small- and large-signal gain [10]. Device processing conditions have been tailored to reduce the impact of fabrication steps (e.g., photolithography, plasma processes) on the surface of the device. Increases in peak power and efficiency associated with such process improvements are believed to stem from changes in the number or behavior of surface electron trapping sites.

IV. Conclusion

Output power density of 12 W/mm was demonstrated from $Al_{0.26}Ga_{0.74}N$–GaN HFETs grown on high-resistivity Si substrates, nearly doubling the previous record power density for any GaN-based FET grown on Si. With a conventional epi structure and device design, these results represent the first demonstration of GaN-on-Si HFETs with performance levels equivalent to state-of-the-art devices grown on sapphire or SiC. Along with the excellent 100-mm uniformity data, these results clearly attest to the viability of high-performance GaN-based electronic devices on low-cost, large diameter Si substrates.

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