

MATERIAL, PROCESS, AND DEVICE DEVELOPMENT OF GaN-BASED HFETs ON SILICON SUBSTRATES

J.W. Johnson, J. Gao, K. Lucht, J. Williamson, C. Strautin, J. Riddle,
R. Therrien, P. Rajagopal, J.C. Roberts, A. Vescan, J.D. Brown,
A. Hanson, S. Singhal, R. Borges, E.L. Piner, and K.J. Linthicum

Nitronex Corporation
628 Hutton Street, Suite 106
Raleigh, NC 27606

Although sapphire (Al_2O_3) and various polytypes of silicon carbide (SiC) have been the most widely employed substrate materials for gallium nitride (GaN) heteroepitaxy, a burgeoning interest in GaN growth on silicon (Si) has emerged in both academic and commercial groups. Historically, the lack of widespread adoption of the GaN-on-Si approach has been attributable to technical challenges presented by the $\sim 17\%$ lattice mismatch and $\sim 56\%$ thermal expansion coefficient mismatch between GaN and Si (111). However, recent efforts have led to stress-relief buffer or transition layer schemes to overcome these limitations, allowing growth of crack-free (Al,Ga,In)N layers on high-quality, low-cost, large-diameter Si substrates (1-3). Other inherent advantages of GaN-on-Si include the ability to leverage well-established Si processing techniques such as wafer thinning, via-hole formation, and AuSi eutectic die attach. A unique feature specific to GaN growth on Si is the possibility to incorporate GaN functionality (e.g., light emission, high breakdown voltage, piezoelectricity) with Si-based devices and circuitry. Although applications requiring integration of these technologies are only beginning to emerge, micro-electromechanical systems (MEMS), chemical sensors, advanced logic, and 3-dimensional integration are a few areas of potential future development.

Third generation (3G) wireless networks represent one of the most promising near-term insertion points for GaN-based electronic devices. AlGaIn/GaN heterostructure field effect transistors (HFETs) have been heavily investigated for use in the output power amplifier stage of 3G basestations, where high linearity and efficiency are critical (4,5). This work will describe development of a vertically-integrated RF power transistor process using a GaN-on-Si platform technology. The process has been optimized for high-linearity performance from 2.11 - 2.17 GHz and targets the 3G wireless infrastructure market. Details of material growth, device fabrication, DC and RF characteristics, and reliability will be given, with an emphasis on novel features of the Nitronex device processing sequence and their impact on transistor performance.

MATERIAL GROWTH

All material was grown on 100 mm float-zone Si (111) substrates in a vertical, cold-wall, metalorganic chemical vapor deposition (MOCVD) reactor. The resistivity of the substrate was $>10 \text{ k}\Omega\cdot\text{cm}$. Growth was nucleated with AlN at 1030°C . A proprietary, strain-compensating (Al,Ga)N transition layer scheme was employed to accommodate mismatch between the substrate and the epilayers. A GaN buffer layer was grown to a thickness of $\sim 0.8 \mu\text{m}$. Proper AlN nucleation conditions and reactor flow dynamics during GaN growth have been shown to play a critical role in overall device performance.

Optimization of these has significantly reduced microwave loss to the substrate (6) and has improved RF power and efficiency of HFETs (7). Various $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layers have been explored, ranging in composition from $x = 0.2$ to 0.3 with barrier thicknesses from 160 - 300 Å. A thin (10 - 50 Å) GaN capping layer was employed on some samples. All layers were nominally undoped. Two-dimensional electron gas (2DEG) sheet resistances of 300 - 350 Ω/\square were measured for HFETs with a 160 Å $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier layer (7).

PROCESS DEVELOPMENT

Conventional GaN FET processing schemes proceed through a sequence of (i) dry etch mesa isolation, (ii) ohmic metallization and anneal, (iii) gate and contact pad metallization, and (iv) passivation. In this type of flow, the channel region of the FET is exposed during all pre-passivation process steps to various photoresist coats, developer solutions, solvents, and plasma descums, as well as effects from the ambient. Since the surface of GaN-based devices -- FETs in particular -- has been shown to be extremely sensitive (8), passivating as early as possible during the device fabrication sequence is an attractive approach. This practice effectively ‘locks-in’ the qualities of the (Al,Ga)N / passivant interface, eliminating unwanted contributions from subsequent process steps. A schematic of an early passivation process flow is given in Fig. 1. Using the early passivation sequence of Fig. 1, this work will demonstrate significant improvements in RF power, efficiency, and reliability over conventionally-processed AlGaN/GaN HFETs operating at 2.14 GHz. Since baseline adoption of the early passivation sequence at Nitronex in mid-2003, an improvement in process stability has also been observed. Similar performance and stability improvements have been previously reported in GaAs pHEMTs (9).

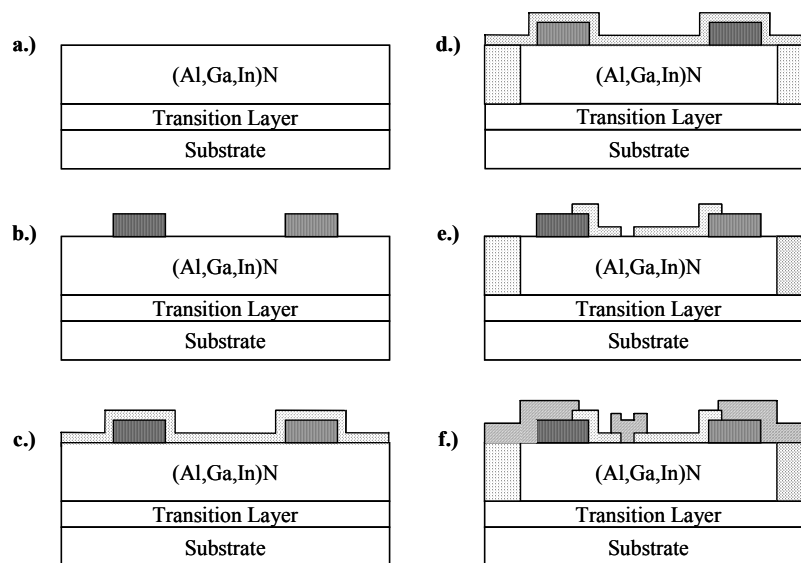


Figure 1. Process flow diagram of early passivation device fabrication sequence. (a.) bare epi; (b.) ohmic metallization and anneal; (c.) PECVD SiN_x passivation; (d.) ion implant interdevice isolation; (e.) ICP SiN_x etch to define gate and contact pad openings; (f.) gate and contact pad metallization.

Device processing began with Ti/Al/Ni/Au (250Å / 1000Å / 400Å / 1500Å) ohmic metallization and RTA in flowing N₂ at ~850°C. Immediately after ohmic anneal, wafers were passivated with a 900Å SiN_x layer. The passivant was deposited at 300°C and 900 mTorr from conventional precursors in a plasma-enhanced chemical vapor deposition (PECVD) reactor. Deposition conditions have been optimized to minimize dispersion and increase RF efficiency in HFETs operating at 2.14 GHz. The passivation step was followed by an ion implantation step to define active areas of the device. Monte Carlo simulations using the Transmission-of-Ions-in-Matter (TRIM) code were used to define conditions of the implant, which was performed through the SiN_x passivant. The simulated vacancy concentration profile of >10²⁰ cm⁻³ from the (Al,Ga)N surface to a depth of ~0.5 μm is shown in Fig. 2. Energy / dose conditions were 30 keV / 6 × 10¹² cm⁻², 160 keV / 1.8 × 10¹³ cm⁻², and (doubly-charged) 400 keV / 2.5 × 10¹³ cm⁻². Typical sheet resistance of implanted material was 10¹¹ Ω/□ and remained thermally stable to 600°C. No post-implant anneal was performed.

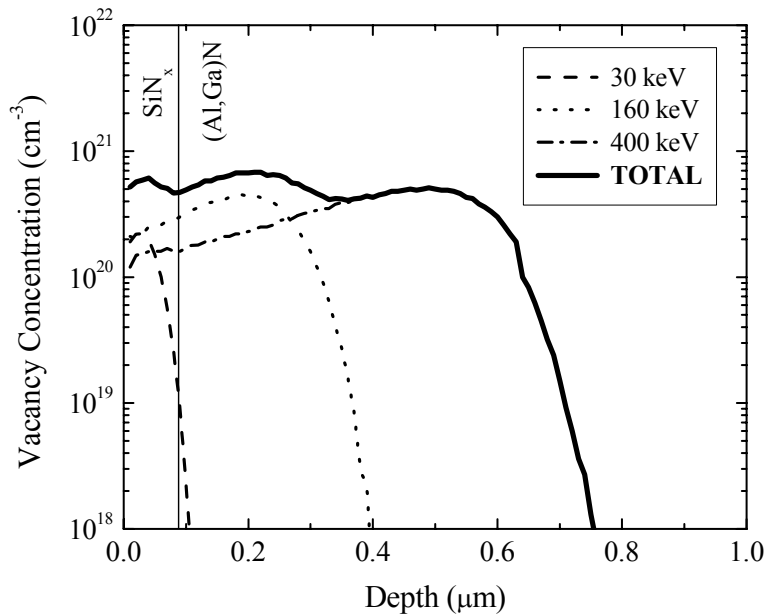


Figure 2. Simulated vacancy distribution from nitrogen ion isolation implant showing SiN_x and (Al,Ga)N layers.

A low-damage SiN_x etch recipe was developed to provide accurate pattern transfer and critical dimension (CD) control for gate openings. High density plasma etch platforms, such as inductively coupled plasma (ICP), are well-suited for this type of etch since their design effectively decouples plasma density from ion energy. Thus, fast etch rates can be obtained without large DC substrate bias. Preliminary process development involved mapping the available parameter space for low-damage, stable plasmas. Chemistries of SF₆, SF₆/O₂ and SF₆/Ar plasmas were explored. Results from unmasked samples indicated that DC bias could be maintained at a very low level while sustaining significant SiN_x etch rates. Figure 3 illustrates etch rate and DC bias as a function of ICP power for 20 mTorr SF₆ plasmas with 5 W RF power. The SF₆ chemistry produced an etch rate of 230 Å/min with DC bias of ~7V at 5 W RF / 100 W ICP. At these

conditions, addition of 5 sccm oxygen increased the etch rate slightly, while addition of 5 sccm of argon decreased the etch rate. Addition of either oxygen or argon increased the DC bias by 1 - 2 V relative to the pure SF₆ chemistry. Investigations of even lower power etch recipes yielded etch rates of ~100Å/min. at 3 W RF power and 60 W ICP power with a 20 sccm flowrate of SF₆. This recipe was used for all structures described in the remainder of this work.

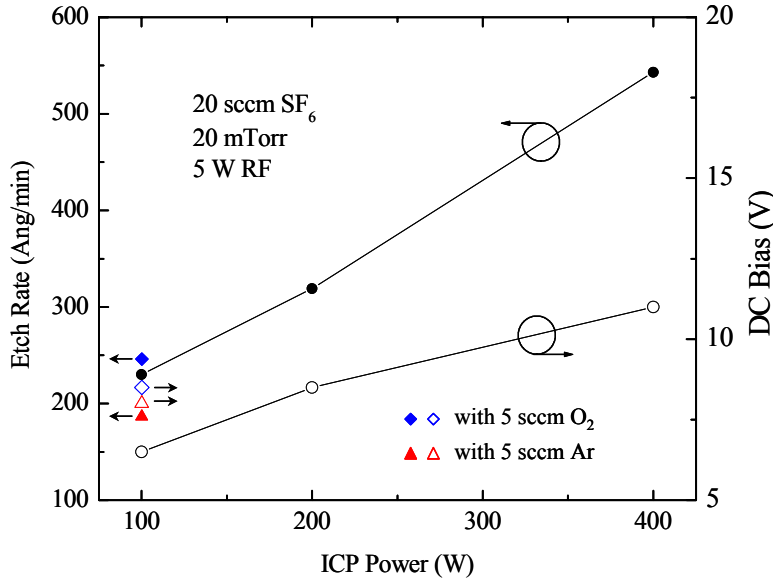


Figure 3. SiN_x etch rate as a function of ICP power for a fixed RF power of 5 W. Note the simultaneous attainment of high etch rate and low DC bias.

To ensure adequate yield, excellent uniformity of both the PECVD SiN_x deposition and the ICP etch rate is required across the wafer diameter. Figure 4 gives 25-point uniformity maps of (a.) as-deposited SiN_x thickness and (b.) SiN_x thickness after a partial ICP etch of an unpatterned wafer. The mean thickness of the as-deposited layer was 3060 Å with a standard deviation of 5.8 Å (± 0.3% uniformity). After ICP etch, the thickness was 1811 Å with a standard deviation of 7.2 Å (± 0.6% uniformity). Despite the excellent uniformity of the PECVD and ICP steps, a certain amount of overetch is typically desired to ensure process robustness. To assess the impact of overetch on characteristics of the gate contact, plasma exposure experiments were performed. These experiments were intended to magnify any plasma-induced surface damage to the underlying (Al,Ga)N upon completion of the SiN_x etch. Unpassivated devices with photoresist openings in the gate region were exposed to an SF₆ plasma for 10 minutes (Fig. 5, inset). After plasma exposure, Ni/Au gates were deposited by e-beam evaporation. Control devices were fabricated without plasma exposure. Gate I-V characteristics were collected from plasma-exposed and control devices and are shown in Fig. 5. Both sets of devices were unpassivated. The excellent agreement between the turn-on behavior of the gate diodes clearly indicates that no surface damage has occurred. Reverse I-V characteristics of plasma-exposed and control samples were also very similar. It should be noted that (Al,Ga)N is impervious to SF₆ at these energies (i.e.,

none of the III-N material was etched by the plasma). The Schottky barrier height and ideality factor extracted from the data shown in Fig. 5 are $\phi_B = 1.06$ eV and $n = 1.25$.

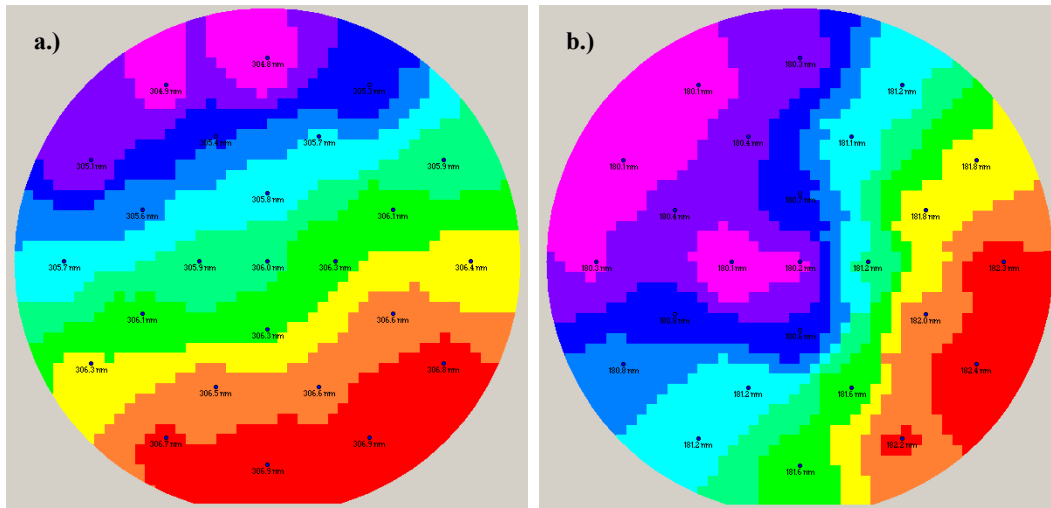


Figure 4. Thickness contours of (a.) ~ 3000 Å PECVD-deposited SiN_x layer and (b.) the same layer after partial ICP etching in an SF_6 plasma. The uniformity of the as-deposited and etched layers are $\pm 0.3\%$ and $\pm 0.6\%$, respectively, across the 100 mm substrate.

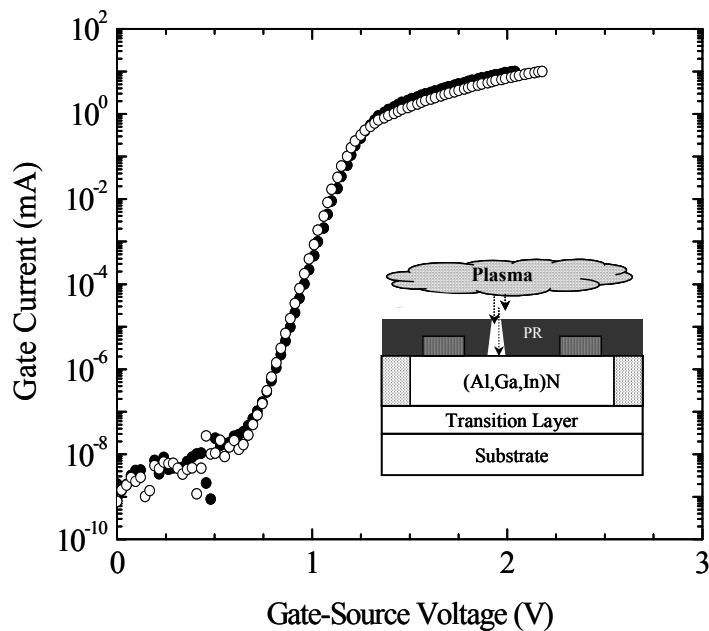


Figure 5. Forward gate I-V characteristics of plasma-exposed (\circ) and control (\bullet) samples used to assess damage from the ICP SiN_x etch process. The excellent agreement between the curves indicates no plasma-induced surface damage to the $(\text{Al,Ga})\text{N}$.

I-line stepper lithography and a thin, positive-tone photoresist etch mask were used to create openings for the gate SiN_x etch. A resist coat of 0.5 - 0.6 μm demonstrated excellent selectivity to the SiN_x during ICP etching. This is in part attributable to the minimal physical component of the low-bias etch process. An SEM micrograph taken after ICP SiN_x etch but before photoresist removal is shown in Fig. 6. Note that the SiN_x etch is rather isotropic, undercutting the photoresist by 0.05 μm on each side. However, this leads to two very advantageous features: (i) excellent CD transfer from the bottom of the PR mask to the bottom of the SiN_x (which will determine the gate length) and (ii) a SiN_x sidewall profile suitable for subsequent gate metal evaporation. The nominal gate length and the measured dielectric opening for the device of Fig. 6 were 0.7 μm and 0.69 μm , respectively, clearly illustrating excellent CD control. The process has been used to produce gate resolution to 0.5 μm .

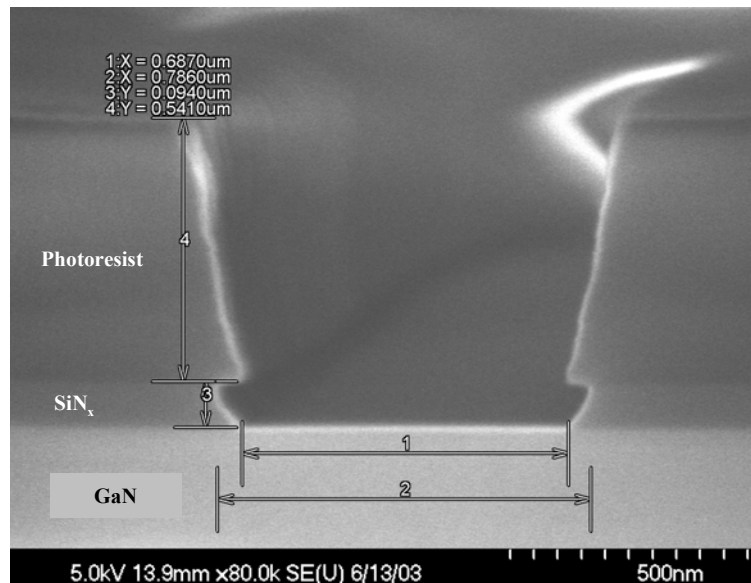


Figure 6. Cross-sectional micrograph of gate region immediately after gate length-defining SiN_x ICP etch. The nominal gate length was 0.7 μm . The sloped sidewalls are suitable for subsequent gate metallization.

Schottky gates of Ni/Au (200 \AA / 5k \AA) were defined using a separate lithography step to allow overlap of the gate metallization onto the surface of the passivant, forming a dielectrically-defined T-gate, as shown schematically in Fig. 1f. Forming the sidewalls of the gate electrode within the SiN_x layer also avoids certain problems associated with trapezoidal gates from conventional lift-off processes. Scanning tunneling electron microscopy (STEM) was used to image cross-sections of both trapezoidal and dielectric T-gates with the same Ni/Au metallization (Fig. 7a and 7b). The trapezoidal gate exhibited a severely tapered profile at both edges with Au ‘spillover’ at the edges of the contact, leading to both Ni and Au contacting the underlying (Al,Ga)N. These effects were not eliminated by increasing throw distance in the evaporation system or by the use of metal interlayers such as Ti between the Ni and Au. As evidenced by Fig. 7b, the T-gate leads to a continuous, constant-thickness layer of Ni as the Schottky barrier metal. Two-dimensional electric field simulations at the drain edge of the gate electrode were performed to evaluate the effect of gate sidewall profile near the semiconductor surface. Figs. 7c and 7d illustrate the fields established within the device for a drain-source

voltage (V_{ds}) of 28 V and a gate-source voltage (V_{gs}) of 0 V. The gate-drain spacing used in the simulation was 3 μm . Clear differences in the electric field profile are noted between the trapezoidal gate (Fig. 7c) and the dielectrically-defined T-gate (Fig. 7d). The peak electric field for the trapezoidal gate was 6.4×10^6 V/cm. This value was reduced to 2.4×10^6 V/cm (reduction of $>60\%$) for the T-gate shown in Figs. 7b and 7d. The field lines are also more clearly distributed in Fig. 1d, illustrating a “nano field-plating” effect at the surface of the semiconductor.

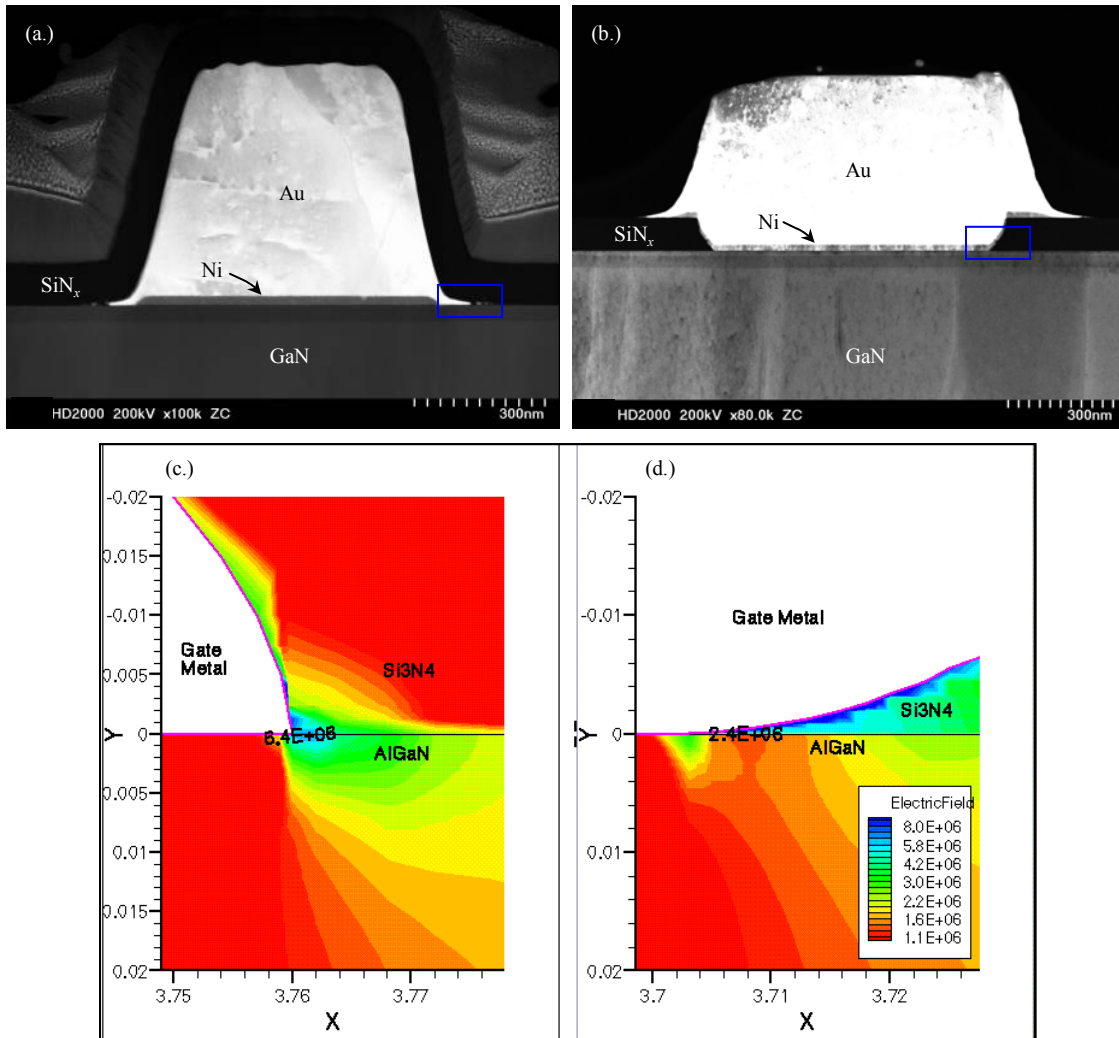


Figure 7. Cross-sectional micrographs of (a.) standard trapezoidal gate and (b.) dielectrically-defined T-gate. The electric field distributions for the highlighted areas (drain side of gate) are given in (c.) and (d.). Dimensions of the X and Y axes are given in microns. Simulations were performed at $V_{ds} = 28$ V and $V_{gs} = 0$ V.

The HFET process sequence was completed by PECVD deposition of a thick SiN_x encapsulation layer and interconnection of large periphery devices using electroplated Au airbridges. Discrete transistors ranging in size from 0.1 - 36 mm total gate width have been fabricated and characterized.

DEVICE CHARACTERIZATION AND PERFORMANCE

Maximum drain current ($I_{D,max}$) uniformity contours from a 100 mm $Al_{0.26}Ga_{0.74}N/GaN$ HFET wafer processed with the early passivation sequence are shown in Fig. 8. Drain current values from 69 test sites across the wafer are shown, resulting in a mean $I_{D,max}$ of 1036 ± 42 mA/mm. The $I_{D,max}$ point is defined as the drain current at which the forward gate current becomes 1 mA/mm. This typically occurs at $V_{gs} \approx 2.5$ V. For the wafer shown in Fig. 8, peak extrinsic transconductance was 285 ± 9 mS/mm for $0.7 \mu m \times 100 \mu m$ devices. Three-terminal drain leakage current at $V_{ds} = 150$ V and $V_{gs} = -8$ V was ~ 0.3 mA/mm. At low voltage, leakage current was similar for early passivation and conventionally-processed devices, but catastrophic breakdown voltage was superior for early passivation devices. This is likely due to localized field-crowding at the drain edge of the gate electrode in trapezoidal gate devices, as shown in Fig. 7c.

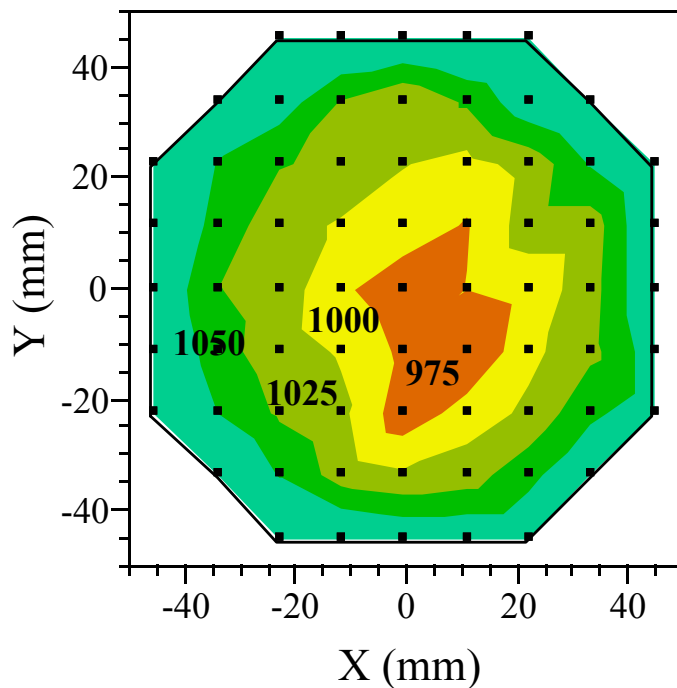


Figure 8. Maximum drain current contour plot for 69 test sites across a 100 mm wafer. The mean drain current density is 1036 mA/mm.

On-wafer large-signal measurements were collected at a frequency of 2.14 GHz using Focus Microwaves mechanical tuners and HFETs ranging in size from 0.1 - 2 mm. The wafer stage was maintained at a constant temperature of 25°C during all measurements. Significant differences between conventionally-processed and early passivation devices were noted in both saturated output power (P_{sat}) and power-added efficiency (PAE). An experiment was performed using 7 $Al_{0.21}Ga_{0.79}N/GaN$ wafers from sequential epi growths. From this sequence, wafers 1, 3, and 5 were processed using a conventional process flow and wafers 2, 4, 6, and 7 were processed with the early passivation flow. Power density results, normalized to remove a systematic drift from the epi process, from $2 \times 0.7 \mu m \times 150 \mu m$ HFETs biased at $V_{ds} = 15$ V and $I_{dq} = 25\%I_{D,max}$ are shown in Fig. 9. A clear difference between the 2 processes is noted. Specifically, a $\sim 20\%$ increase in saturated output power is achieved with the early passivation process.

A similar plot (not shown) demonstrated an improvement in PAE of 3 percentage points. Gain was ~ 0.4 dB higher for the trapezoidal gate device, presumably due additional gate capacitance from the T-gate structure.

The mechanism for the improvement in power density and efficiency for the early passivation process almost certainly involves surface traps. Since surface traps have been demonstrated to reduce power and efficiency in GaN-based FETs (8), the differences noted in Fig. 9 are consistent with a change in the number or dynamics of active trapping sites on the (Al,Ga)N surface. As described previously, the act of passivating early in the device fabrication sequence minimizes surface exposure to process chemistries, plasmas, and the atmosphere. This could lead to a reduction in the number of surface traps or a change in the trap energy distribution(s). Alternatively, Fig. 7 illustrated that the early passivation process leads to a T-gate electrode that alters the electric field established at the drain edge of the gate. Since the most likely supply of electrons to surface trapping sites is the reverse-biased gate electrode, a change in the field profile (i.e., the driving force for electron injection from the gate) may reduce the *supply* of electrons to surface traps. For either mechanism, the early passivation process appears preferable.

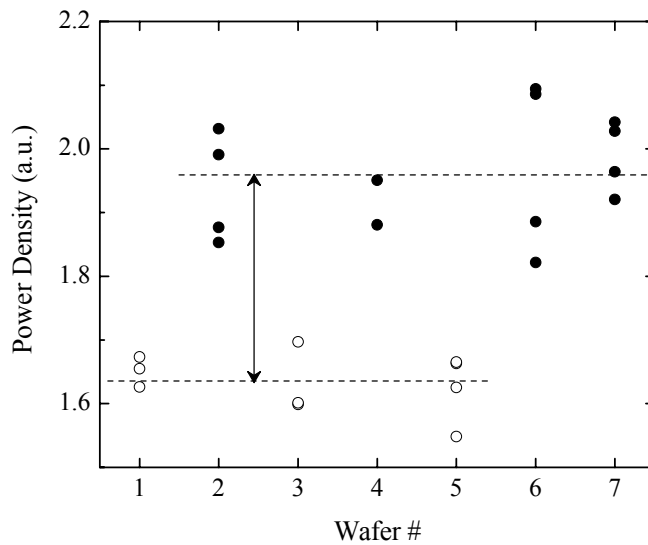


Figure 9. Power density comparison between conventional process flow (○) and early passivation flow (●) for 300 μm gate width devices. The early passivation process improved power density by $\sim 20\%$.

Epi structures consisting of a 160\AA $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier layer were processed with the early passivation flow. The devices gave DC performance similar to the data of Fig. 8. Load pull measurements were performed on wafers thinned to $150\ \mu\text{m}$ and backmetallized with Au. A 2.14 GHz CW power sweep from a $2 \times 0.7\ \mu\text{m} \times 50\ \mu\text{m}$ HFET is shown in Fig. 10. The device was biased at $V_{\text{ds}} = 40\ \text{V}$ ($I_{\text{dq}} = 0.22\ \text{A/mm}$) and was manually tuned for a power / efficiency figure of merit. The measured output power of 30.45 dBm corresponds to a power density of 11 W/mm. Small-signal gain and peak PAE were 22 dB and 65%, respectively. These results represent, to the best of the

authors' knowledge, the best combination of power and efficiency ever obtained from a GaN device on a silicon substrate and compare favorably with state-of-the-art results from devices on any substrate.

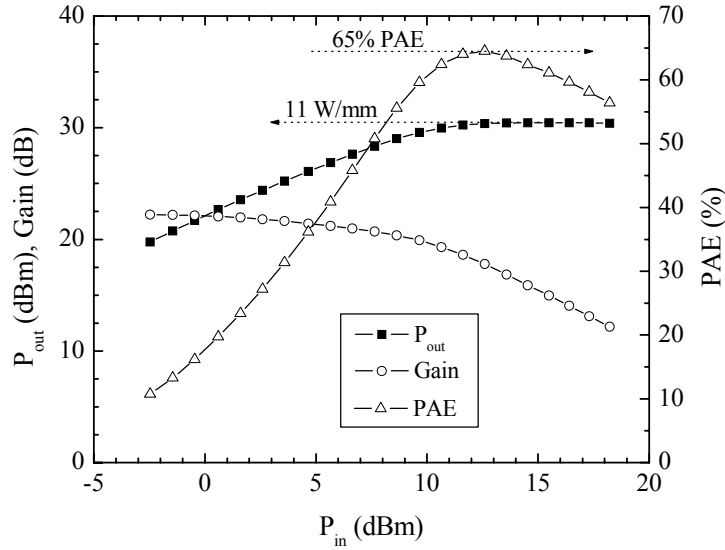


Figure 10. 2.14 GHz CW power sweep of a 100 μm gate width Al_{0.26}Ga_{0.74}N/GaN HFET. Bias conditions were $V_{ds} = 40$ V and $I_{dq} = 22$ mA.

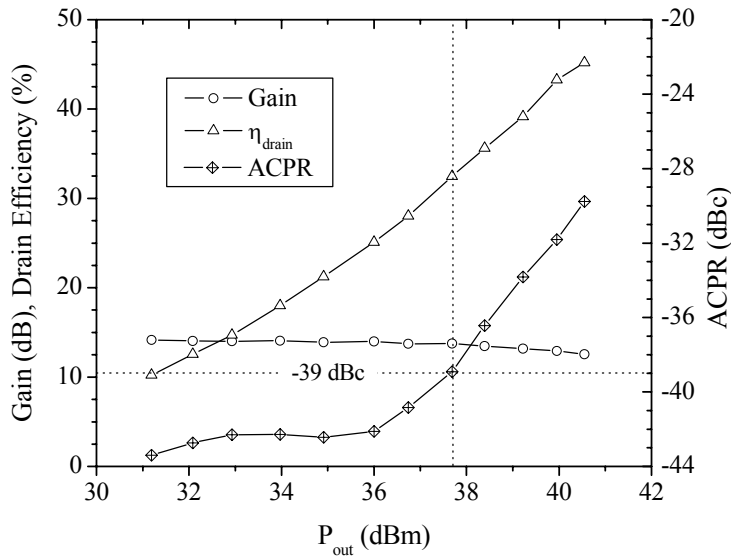


Figure 11. ACPR characteristics of a packaged 16 mm HFET with no internal matching. The device produced 5.7 W of linear power at an adjacent channel power ratio of -39 dBc. At this linearity condition, $\eta_{drain} = 31\%$ and gain = 13.5 dB.

In addition to RF performance improvements under CW modulation, early passivation has been shown to produce improvements in linear power characteristics. Sixteen millimeter gate periphery ($80 \times 200 \mu\text{m}$) devices were packaged without internal matching and were tested using a W-CDMA modulated signal (Test Model 1 with 64 users, 100% clipping, PAR of 8.5 dB @ 0.1% probability and 9.8 dB @ 0.01%). Performance is shown in Fig. 11. At $V_{ds} = 28 \text{ V}$ and an adjacent channel power ratio (ACPR) of -39 dBc, the power density was 350 mW/mm, producing a total of 5.7 W of linear output power from the 16 mm device. The ACPR plateaued at approximately -44 dBc and did not exhibit a local minimum. Drain efficiency and gain at -39 dBc were 31% and 13.5 dB, respectively. For comparison, conventionally-processed 16 mm devices from the same material structure yielded output power of $\sim 4.5 \text{ W}$ with drain efficiency of $\sim 25 \%$. Tuning conditions can greatly affect the tradeoff between gain and efficiency in backed-off W-CDMA operation, and typically one may be sacrificed in order to increase the other. The excellent drain efficiency is extremely attractive for basestation applications, where it is desired to reduce cooling costs associated with low efficiency amplifiers.

FIELD-PLATED HFETs

The nominal gate metal overhang distance for the early passivation, T-gate process was $0.2 \mu\text{m}$ on each side of the gate stem (Fig. 12, inset), although this process sequence lends itself very well to the formation of field-plated structures. Field plating by dielectric overlap is a well-known technique to reduce field crowding effects at the edge of Schottky contacts, such as the drain edge of the gate electrode of a FET (10). In the early passivation process, field plates can be formed with design degrees of freedom in both metal separation from the semiconductor surface (i.e., passivation thickness) and field plate length (i.e., length of the gate overlap toward the drain). Both of these variables can be used to tailor the electric field profile in the underlying FET. In addition to standard devices with $0.2 \mu\text{m}$ overlap, field-plated structures were formed with overlaps of $0.6 \mu\text{m}$ and $1.2 \mu\text{m}$ toward the drain electrode, maintaining a source overlap of $0.2 \mu\text{m}$. All three of these field plate geometries were fabricated on devices with passivation thicknesses of 450 \AA , 900 \AA , and 1800 \AA , providing a 3×3 field plate design of experiments. Other than leakage current and breakdown voltage, most DC characteristics (e.g., drain current, on-resistance, transconductance, pinchoff voltage) were largely unchanged by the field-plated gates for all passivation thicknesses. As expected, field plating reduced leakage current and increased breakdown voltage in 2 mm FETs. The effect of the field plate length was more pronounced for thinner SiN_x layers, since field-spreading is more pronounced as the field plate is moved closer to the HFET channel. Leakage reduction is illustrated in Fig. 13 for $2 \times 200 \mu\text{m}$ devices with 900 \AA SiN_x thickness. Field-plated devices exhibited lower leakage at all voltages and a reduced sensitivity to voltage (i.e., shallower slope).

Small-signal data were collected to quantify the impact of the T-gate structure on intrinsic FET characteristics, such as gate capacitance. The same effect that leads to field spreading and leakage reduction at DC also typically gives rise to increased gate capacitance and reduced gain at RF frequencies. The scattering parameters were collected using an Agilent 8510C Vector Network Analyzer calibrated to 30 GHz. Gate-drain capacitance (C_{gd}) extracted from a small-signal model is given in Fig. 12 as a function of passivation thickness for each of the field plate geometries. As seen from the

figure, C_{gd} of the standard $0.2\ \mu\text{m}$ overlap gate is about $75\ \text{fF}$, or about 50% higher than for a trapezoidal gate of the same length. The increasing effect of field plate length for thinner SiN_x layers is easily observed from the $450\ \text{\AA}$ data of Fig. 12, where C_{gd} has increased by more than a factor of 7 for a $1.2\ \mu\text{m}$ field plate with $450\ \text{\AA}$ passivant relative to the trapezoidal gate. A result of this gate capacitance increase was a reduction in small- and large-signal gain by 1 - 3 dB, depending on bias conditions, for field plated devices. Still, tradeoffs between gate length and field plates can be used advantageously. For example, a $0.56\ \mu\text{m}$ gate length device with a field plate length of $0.4\ \mu\text{m}$ was biased at $V_{ds} = 15\ \text{V}$ and quiescent bias current (I_{dq}) of 25% $I_{D,max}$ for small-signal measurement. A unity current gain cutoff frequency (f_T) of 20 dB was determined from the $|h_{21}|$ intercept and a maximum frequency of oscillation (f_{max}) of 41 GHz was extrapolated from the maximum available gain using a slope of -20 dB/decade (Fig. 9). The f_{max} / f_T ratio of 2.05 and $f_T \times$ gate length product of $11.2\ \text{GHz}\cdot\mu\text{m}$ attest to the absence of significant substrate charge-coupling effects. The excellent frequency response of the HFET gives clear evidence of the potential for GaN-on-Si devices at frequencies of X-band or higher.

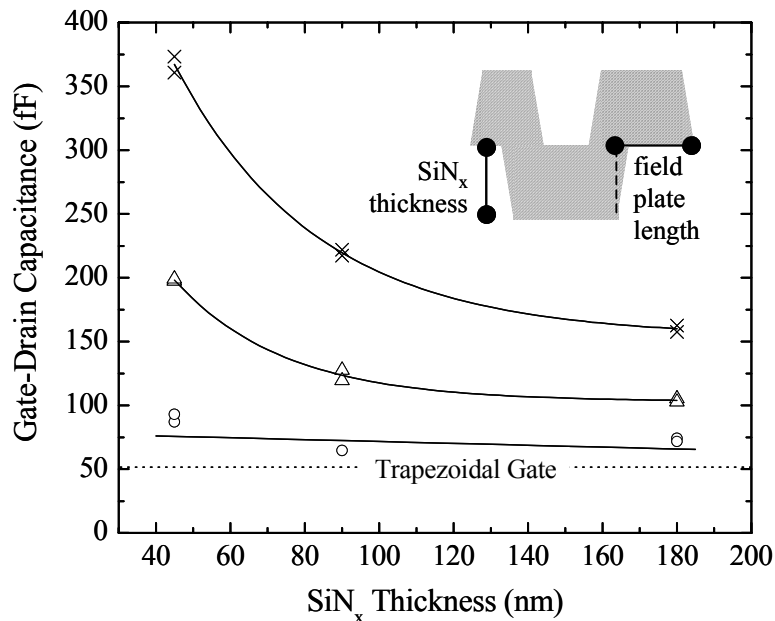


Figure 12. Gate-drain capacitance extracted from small-signal measurements of HFETs with standard $0.2\ \mu\text{m}$ overlap (\circ); $0.6\ \mu\text{m}$ overlap (Δ); and $1.2\ \mu\text{m}$ overlap (\times). Also shown is C_{gd} for trapezoidal gate devices and a schematic of the dimensions available for field plate engineering (inset).

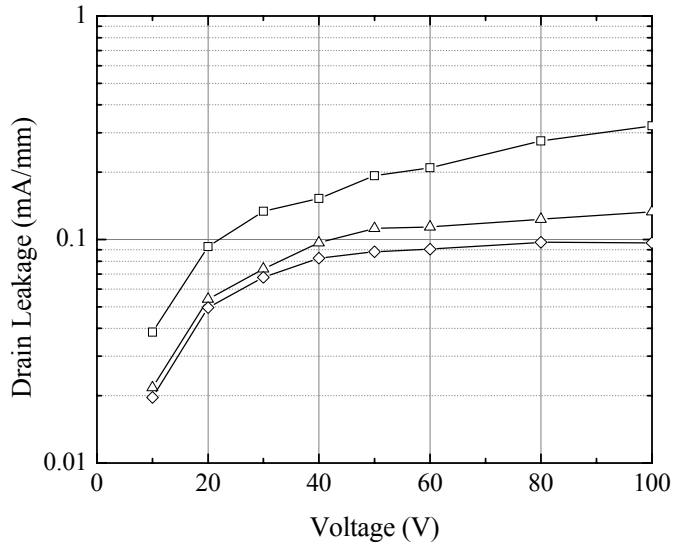


Figure 13. Two-terminal leakage current sweep collected from the gate-drain diode of a 2 mm HFET with 0.2 μm overlap (\square); 0.6 μm overlap (\triangle); and 1.2 μm overlap (\diamond).

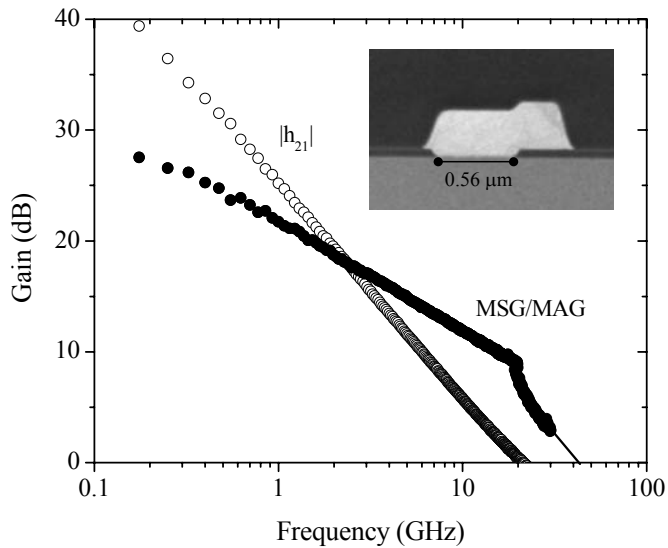


Figure 14. HFET small-signal characteristics at $V_{ds} = 15\text{V}$. The f_T and f_{max} of the device were 20 GHz and 41 GHz, respectively. Also shown is a cross-section of the 0.56 μm gate with 0.4 μm field plate from this device.

RELIABILITY

Before insertion of GaN-based devices into commercial or military systems, excellent reliability must be clearly demonstrated. This work is gaining considerable momentum at various research and development centers, but is still in early stages of

characterization. At Nitronex, DC burn-in is used to monitor early-life performance drift, extrapolate lifetime estimates, and to stabilize performance metrics of packaged parts from every processed wafer. The early passivation approach led to a favorable change in the nature of the DC burn-in behavior relative to conventionally-processed devices. DC burn-in was performed on 16 mm packaged devices with no internal matching (Fig. 15, left inset), similar to those used to generate the data in Fig. 11. The packaged parts were mounted into test boards to produce a $50\ \Omega / 50\ \Omega$ environment. The 16 mm devices were biased at $V_{ds} = 28\ \text{V}$ and the gate voltage was tuned to give $I_d = 1.3\ \text{A}$. From thermal simulations, this bias condition provides a junction temperature of $\sim 200^\circ\text{C}$. Figure 15 (left) shows the difference in the 24-hour burn-in behavior between the 2 device fabrication sequence. Note that the initial ($\sim 2\ \text{hr.}$) current drop was similar, but that the early passivation device stabilized very quickly relative to the conventionally-processed device. In fact, the early passivation device appears to have completely stabilized by $t = 12\ \text{hrs.}$ The conventionally-processed device continued to degrade monotonically throughout the burn-in. Extrapolation of these data on a log-normal scale gave an estimate of the drain current drift that may be expected over operating life (Fig. 15, right). To 10^5 hours, the drain current of the conventionally-processed device is expected to decrease by 300 mA, or more than 20%. Conversely, I_d of the early passivation device is predicted to decrease by $\sim 5\%$. From 1500 hour DC-stress data, extrapolation of 16 mm saturated power density over a 20-year operating life gave ΔP_{sat} of only -0.88 dBm.

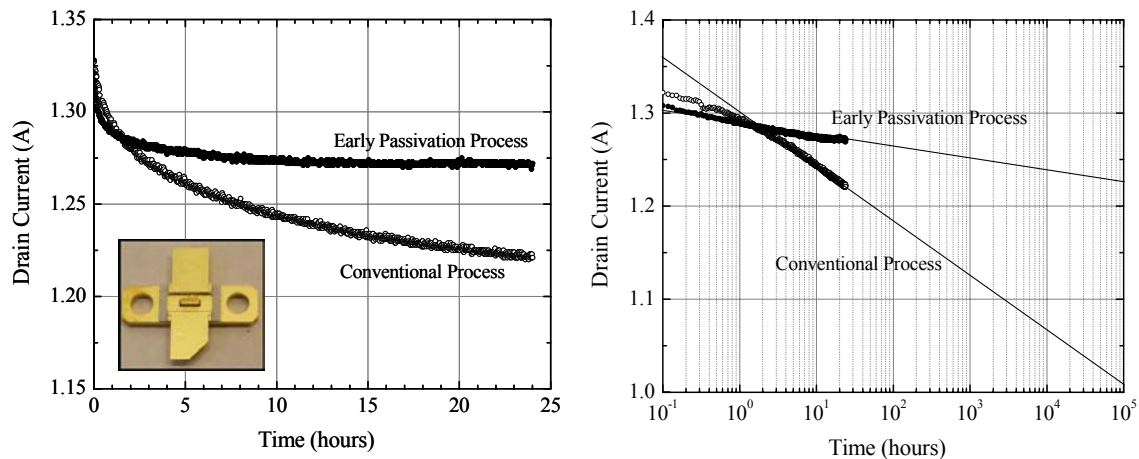


Figure 15. 24-hour DC burn-in curves illustrating I_d drift (left) and extrapolation of I_d drift to 10^5 hours (right). Note the significant impact of device fabrication sequence on reliability performance. A packaged 16 mm HFET is shown in the inset.

CONCLUSION

A device fabrication sequence has been developed in which a SiN_x passivant is deposited very early in the process flow. A low-damage ICP etch recipe was used to define openings in the SiN_x layer for subsequent gate metallization. The fluorine-based etch demonstrated excellent uniformity and critical dimension control across 100 mm substrates. The resultant dielectrically-defined T-gates allowed creation of field-plated structures, which were shown to reduce leakage but increase gate capacitance. Small

periphery devices fabricated with the early passivation process yielded 11 W/mm saturated output power with 65% peak PAE, representing the current state-of-the-art for GaN-on-Si FETs. Linearity performance of packaged 16 mm HFETs also improved with the early passivation approach. A 16 mm device biased at 28 V demonstrated >30 % drain efficiency at an ACPR of -39 dBc under W-CDMA modulation. The ability of GaN-on-Si HFETs to operate at frequencies above S-band was demonstrated by f_T and f_{max} values of 20 GHz and 41 GHz, respectively, for a 0.56 μm gate length device. Improvements in DC burn-in performance were shown and a drain current drift of ~5% was extrapolated for a 10^5 hour operating life.

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