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AlGaN/GaN HFETs on 100 mm Silicon Substrates for Commercial Wireless Applications

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GaN grown on Si is currently the only pathway towards high volume manufacturing of GaN based RF devices. In this paper we present the technological status of GaN grown on 100 mm Si substrates. Optimised growth, accounting for the lattice and thermal coefficient of expansion mismatch results in device quality GaN layers that exhibit excellent uniformity over the 100 mm Si substrate. The electrical characteristics of the fabricated devices reflect the high quality of the layers, leading to saturated power levels of 3.3 W/mm, the highest power densities reported to date for GaN on Si. Large periphery devices are shown to achieve up to 27 W of output power.

Introduction The outstanding potential of group III-nitride heterostructure FETs has been repeatedly demonstrated in a wide frequency range, showing a tenfold improvement over "conventional" semiconductors like Si or GaAs in terms of power density [1, 2]. This performance is mainly due to the ability of GaN based devices to operate at high drain voltages while simultaneously yielding high two-dimensional electron gas (2DEG) carrier densities.

Currently, base station power amplifiers for wireless communication at L-band are being driven by Si-based LDMOS transistors. Serious limitations of Si LDMOS technology have been shown however, especially for the next generation communications standards, which require higher power and operating voltage levels and significantly improved linearity. GaN based devices have the potential of delivering RF signals with significant improved linearity [3, 4]. Up to now, and also for the foreseeable future [5] no GaN or AlN substrates are commercially available in practical sizes. Therefore, the majority of results have been achieved on sapphire or SiC substrates, where epitaxial growth techniques have been developed to address the challenge of the large lattice mismatch.

The commercial success of GaN-based RF devices is going to be dependant on manufacturability details, such as backside processing capability, thermal conductivity, substrate resistivity, defects, and most importantly the size and price of the substrate. In this presentation we will demonstrate the viability of GaN on Si, offering a low cost large area technology, hence opening the pathway for commercial application of GaN-RF devices.

Materials Technology Using Si as a substrate material for GaN based devices enables a variety of applications and manufacturing technologies. The 100 mm Si substrate platform allows use of larger state-of-the-art compound semiconductor and silicon manufac-

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turing tools standard to the semiconductor industry to be used. The wide availability of Si substrates of different conductivity types (n-, p-, and high resistivity) enables both vertical devices (LEDs, laser diodes, HBTs, high power switches) and RF components. In addition, the thermal conductivity, comparable to that of GaN, provides a more relaxed thermal budget as compared to sapphire substrates. However, due to the lattice mismatch of 20% and the large difference in thermal expansion coefficients, the growth of GaN on Si is much more challenging than on sapphire or SiC. This can lead to cracking of the GaN layers, seriously limiting the thickness of the GaN film. Several groups have employed different approaches to overcome this problem, using buffer structures including AlN, superlattices, and lateral overgrowth, for example [6–8].

Our GaN epitaxy on Si is based on a multi-injector MOCVD system design, scaled for growth on 100 mm Si substrates. A proprietary SiGaNtic process was developed to accommodate the lattice and the thermal expansion coefficient mismatch between GaN and silicon, which produces uniform crack-free GaN films with thicknesses exceeding 2 μm. The SiGaNtic approach utilizes an (Al,Ga)N based transition layer with a proprietary composition and growth-condition profile [9].

With routine growth of crack-free GaN established, efforts were undertaken to produce device quality AlGaN/GaN heterostructures by optimisation of growth conditions. The material quality and uniformity of these 100 mm HFET wafers were characterized by a wide variety of techniques including XRD, thickness measurement, photoluminescence spectroscopy, Hg probe C–V profiling, reflectance spectroscopy, AFM, SIMS, Hall and sheet resistance measurements. Many of these measurements were mapped across the 100 mm wafer to validate the uniformity of the growth process. The AlGaN/GaN HFET structures characterized by the above techniques are of device quality and comparable to AlGaN/GaN structures grown on SiC or sapphire. These material properties are presented below.

The ability of growing uniformly thick III-nitride layers was the first step in developing a viable GaN buffer for the AlGaN/GaN HFETs. The dislocation density of these GaN layers is $\approx 2 \times 10^9$ cm^{-2} and X-ray diffraction spectra reveal a FWHM of 650 arcsec for the GaN (0002) peak. These values of dislocation density and X-ray linewidth validate the effectiveness of transition layer scheme in accommodating the lattice mismatch. As the thickness of the transition layer and epilayers is increased, the RMS roughness of the GaN as determined by AFM can be significantly reduced to levels below 10 Å for a scan area of 5 μm × 5 μm. A high degree of uniformity has been achieved by optimising growth conditions such as reactant flows, temperature and pressure in the multi-zone injection and multi-zone heated MOCVD reac-

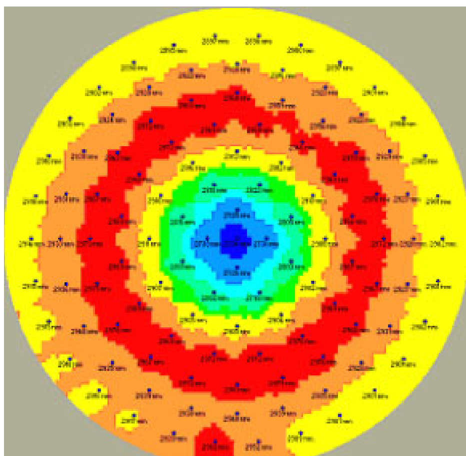

Fig. 1 (online colour). Film thickness map of 2.9 μm GaN on 100 mm Si, with a total thickness variation <10%

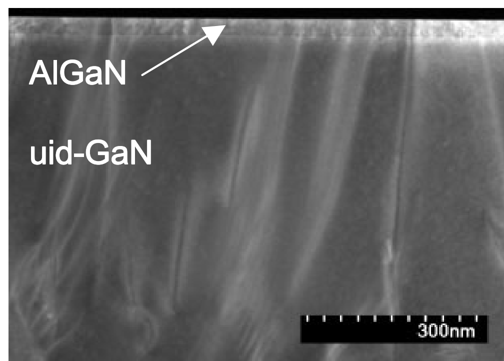

Fig. 2. Cross sectional STEM image of a 21% AlGaN/GaN HFET on 100 mm Si, showing the sharp interface with the GaN buffer

tor. Uniformity improvements were obtained by systematically optimising the parameters that influence reactor flow dynamics and impact recirculation in the growth chamber. The significant parameters were determined to be pressure, temperature, gas injection velocity profile, and rotational speed of the substrate. The uniformity that can be achieved is illustrated in Fig. 1, which shows a Filmetrics map of a 100 mm HFET wafer with a mean thickness of 2.9 μm and <10% total thickness variation (5 mm edge exclusion).

Achieving high performance HFETs critically depends on the electron transport properties in the 2DEG at the AlGaN/GaN interface. Both Hg probe C–V profiling and van der Pauw Hall measurements have been used to assess and monitor the channel characteristics. Growth conditions that led to high quality GaN, AlGaN and smooth, abrupt interfaces were developed, as illustrated in the Scanning Transmission Electron Microscopy (STEM) image in Fig. 2. A key parameter in achieving a smooth and abrupt interface was the fast gas switching in the gas injection manifold and a short residence time of reactants in the growth chamber. Mobilities of 1430–1500 cm^2/Vs, with a sheet charge of $7.6–8.6 \times 10^{12}$ electrons/cm^2 are routinely obtained across a 100 mm diameter $Al_{0.21}Ga_{0.79}N$/GaN HFET wafer. These values are among the best reported for GaN on Si. Presence of the channel is also confirmed by C–V measurements, which show a sharply peaked doping vs. depth profile at a depth consistent with the designed AlGaN thickness of ≈300 Å. Sheet resistance mapping yields a mean value of 530 Ω/square across a 100 mm wafer, with a standard deviation value of 3.7% (5 mm edge exclusion). Room temperature photoluminescence spectra, obtained using a 266 nm pump laser, exhibit sharp band edge emission for both GaN and $Al_xGa_{1-x}N$ peaks. A photoluminescence map of a 100mm $Al_xGa_{1-x}N$ calibration wafer is shown in Fig. 3. The $Al_xGa_{1-x}N$ median peak position is approximately 324 nm, which corresponds to an Al content of approximately 21% (assuming a bowing parameter equal to 1). The standard deviation across the wafer is 1.8 nm, corresponding to 0.556%.

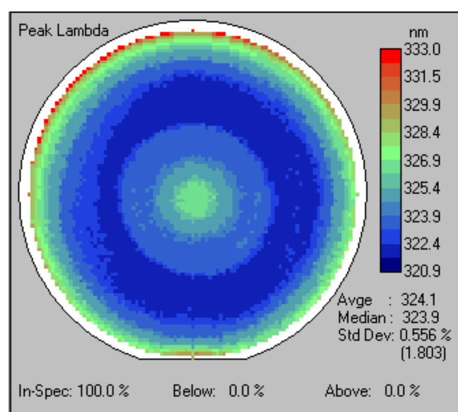

Fig. 3 (online colour). AlGaN PL spectral peak wavelength mapped across a 100 mm HFET wafer. The standard deviation is <0.6%

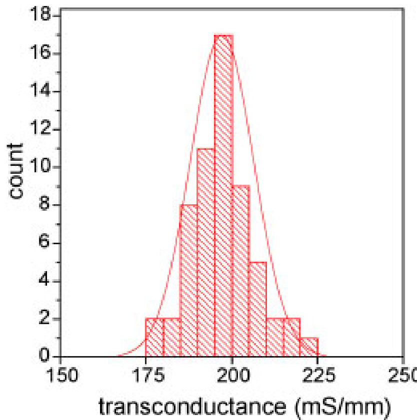

Fig. 4

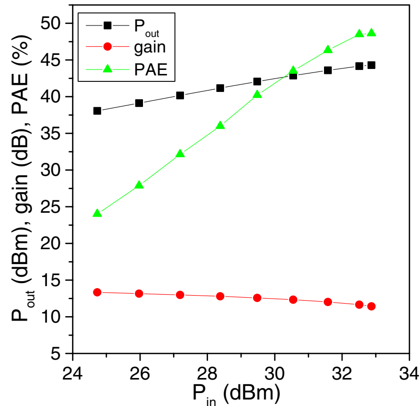

Fig. 5

Fig. 4 (online colour). Transconductance distribution across a 100 m GaN on Si wafer (59 sites, with 5 mm edge exclusion)

Fig. 5 (online colour). Power sweep at 2 GHz, performed on a 18 mm device, yielding 27 W saturated output power

Device Results The HFET structure employed in the process development is a conventional AlGaN/GaN structure, using an undoped GaN buffer layer on top of the transition layer. The active device region is formed by a heterostructure $Al_{0.21}Ga_{0.79}N$/GaN modulation doped heterostructure terminated by a GaN cap layer. Standard GaN processing techniques are employed for the device fabrication, with Ti/Al based Ohmic contact, 0.7–1.0 μm Ni/Au gates defined by stepper lithography and Au interconnects for multi-finger devices. Typically, small periphery device performance is mapped and measured on-wafer and is used for process control as well as material device correlations. The electrical properties reflect the excellent uniformity of the epitaxial materials as well as the process control. Figure 4 shows the distribution of the transconductance (gm) across a 100 mm wafer. Out of 62 sites tested 59 sites yielded functional devices. The mean value of gm was at 197 mS/mm with a standard deviation of <10 mS/mm.

Power measurements are typically performed on-wafer at 2 GHz on 300 μm devices. Operated at a drain bias of 30 V saturated power densities up to 3.3 W/mm were achieved, the highest number ever reported for a GaN on Si transistor. For viable commercial applications, large periphery devices with high absolute power levels need to be developed. We have fabricated large periphery devices with up to 18 mm total gate width (90 fingers of 200 μm each). These devices were packaged in standard RF packages. At a gate length of 1 μm, power measurements performed at 28 V drain bias yields a saturated power of up to 27 W with a maximum power added efficiency (without harmonic tuning) of 48% (Fig. 5).

Conclusion We have shown the status of materials and device performance of GaN grown on 100 mm Si substrates. Excellent epitaxial material quality and uniformity ensure high yield device performance. The electrical performance (with up to 3.3 W/mm saturated output power on small devices, as well as up to 27 W on packaged die) demonstrates the viability and readiness of this technology for commercial processing and fabrication.

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