



150W GaN-on-Si RF Power Transistor

Walter Nagy
wnagy@nitronex.com
919-807-9100 ext 141

Outline

>> Device Design

- ▶ Why GaN?
- ▶ HFET Device Structure
- ▶ Device Design
- ▶ RF Results - CW, WCDMA, DPD
- ▶ Reproducibility
- ▶ Benefits of Higher Voltage
- ▶ Thermal Optimization

>> Reliability Data

- ▶ Reliability Test Plan
- ▶ Baseline Control Chart
- ▶ Reliability Status

>> Summary

Why Gallium Nitride?

Attribute	Si	GaAs	SiC	GaN
Energy Gap (eV)	1.11	1.43	3.2	3.4
Critical Electric Field (MV/cm)	0.6	0.65	3.5	3.5
Power Density (W/mm)	~ 0.8	~ 1.0	2 - 4	> 2
Saturation Velocity (cm/s)	1x10 ⁷	2x10 ⁷	2x10 ⁷	2.5x10 ⁷
FET Technology	LDMOS	HFET	MESFET	HFET

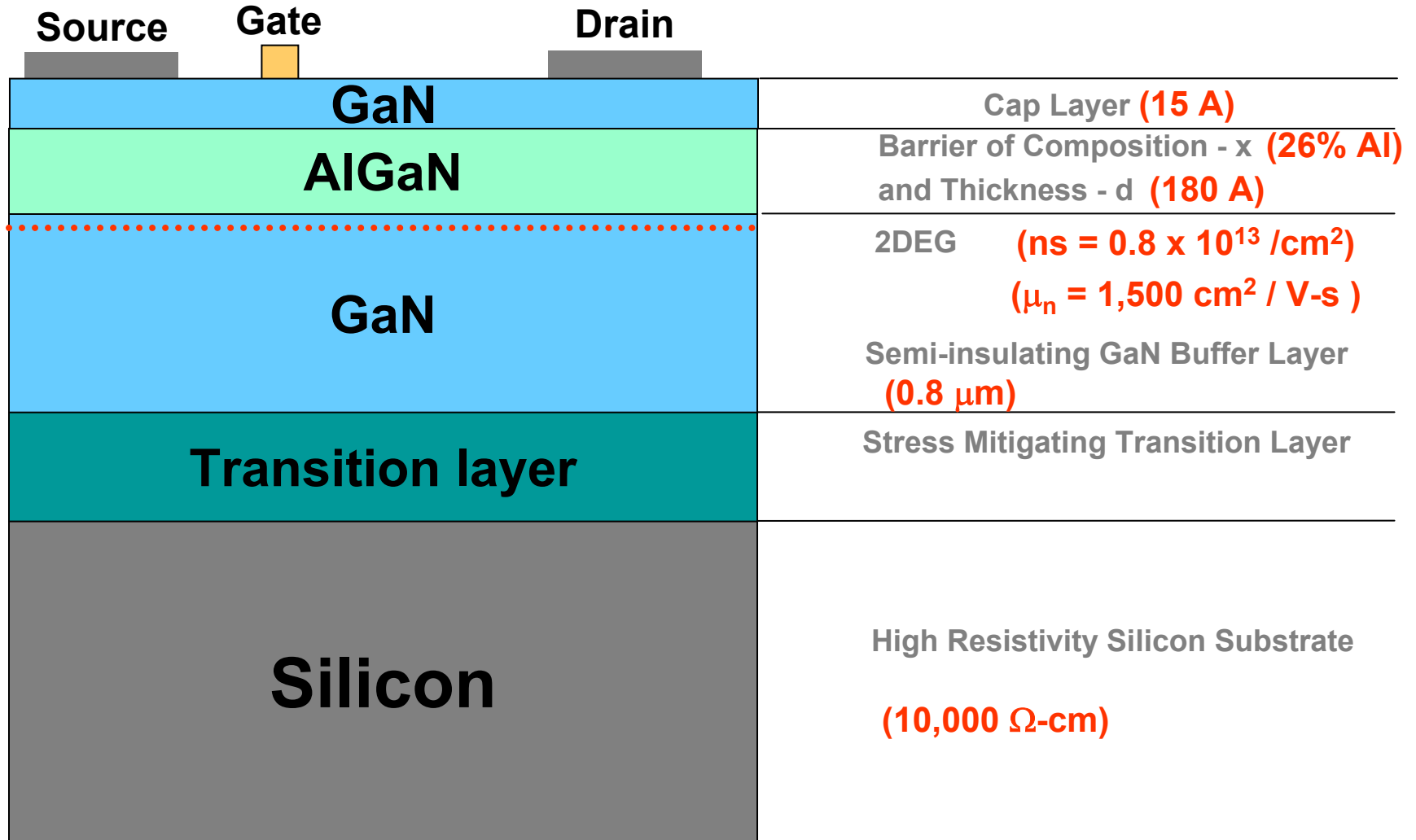
High Voltage

High Power Density

High Frequency

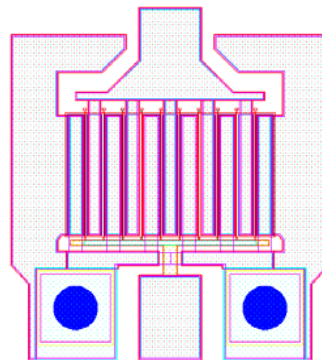
GaN = best material attributes for microwave power applications

HFET Device Structure



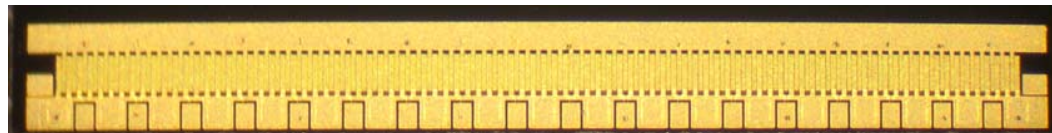
Building Block Chips

Unit Cell (On-Wafer Probable)



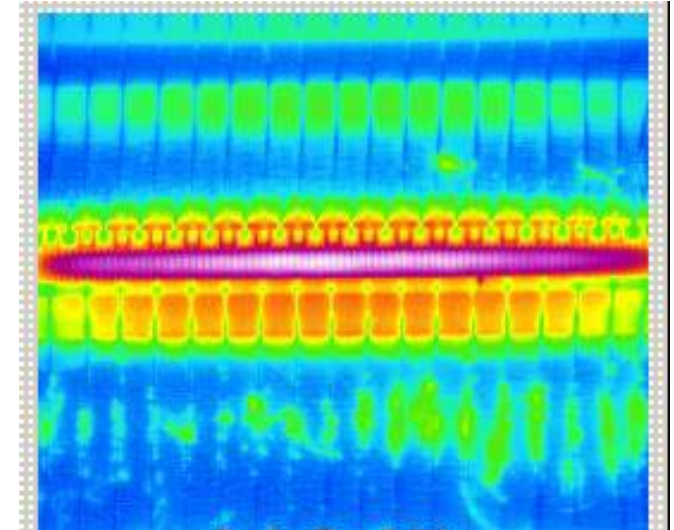
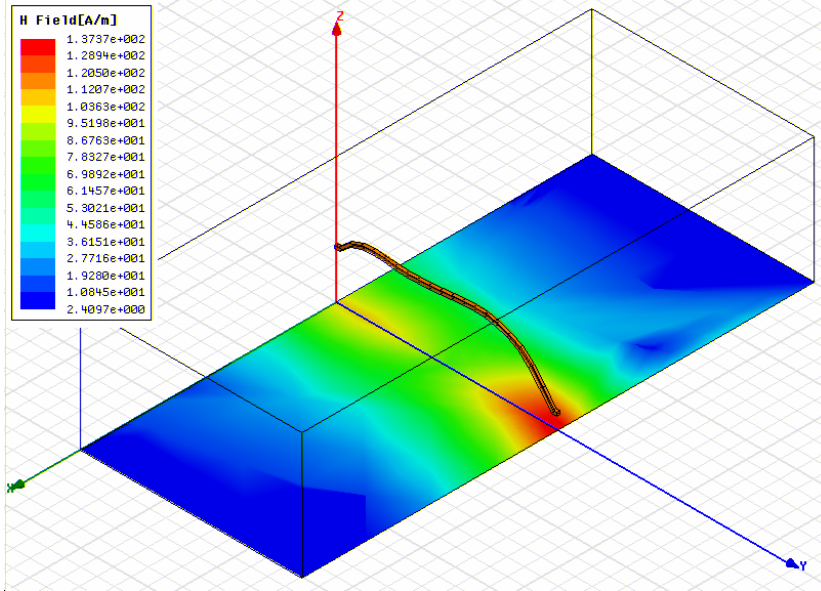
- Gate Periphery = 2mm (10 x 200 μm)
- $P_{\text{sat}} = 5 - 6 \text{ W @ } 28\text{V}$
- Peak Efficiency = 60 - 65%
- Linear Gain = 19 dB
- $Z_s \sim 14 + j 3$
- $Z_l \sim 53 + j 59$

Power Chip (1mm X 6mm)



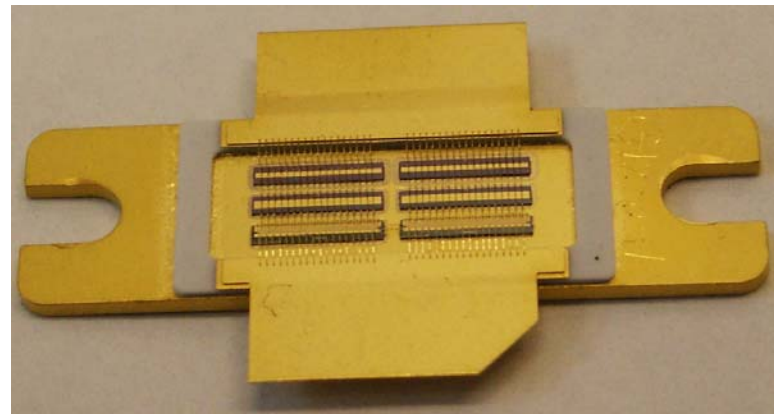
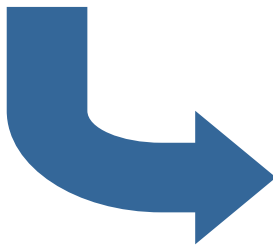
- Gate Periphery = 36mm (18 cells)
- $P_{\text{sat}} = 70 - 80\text{W @ } 28\text{V}$
- Peak Efficiency = 60 - 65%
- Linear Gain = 15 - 16 dB

Internal-Matching Design



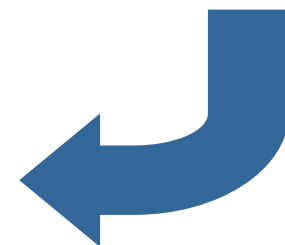
Design and Modeling

- Bondwire Modeling
- Cell Scaling
- Network Design



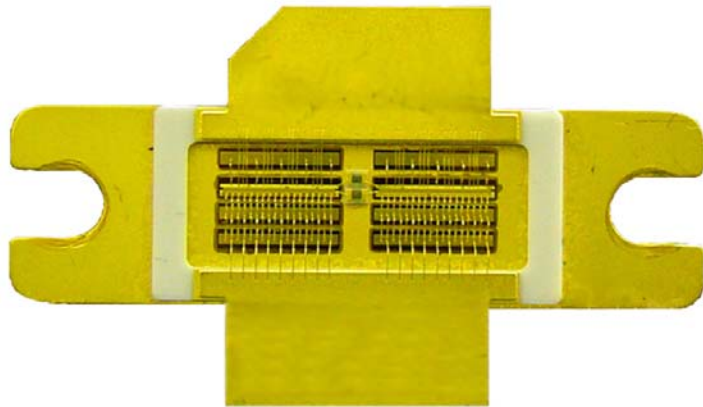
Characterization

- IR Scans
- Load-Pull
- Pulsed DC



150W RF Power Transistor

- Two 36mm GaN die in CuW ceramic package
 - ▶ Internal matching networks
 - “PI” input network
 - “TEE” and “Shunt L” output network
 - ▶ 28 VDC, 7% Idss, 2.14 GHz
 - $Z_s=3-j4$ ohms, $Z_l=3-j4$ ohms



2 X 36 mm Device

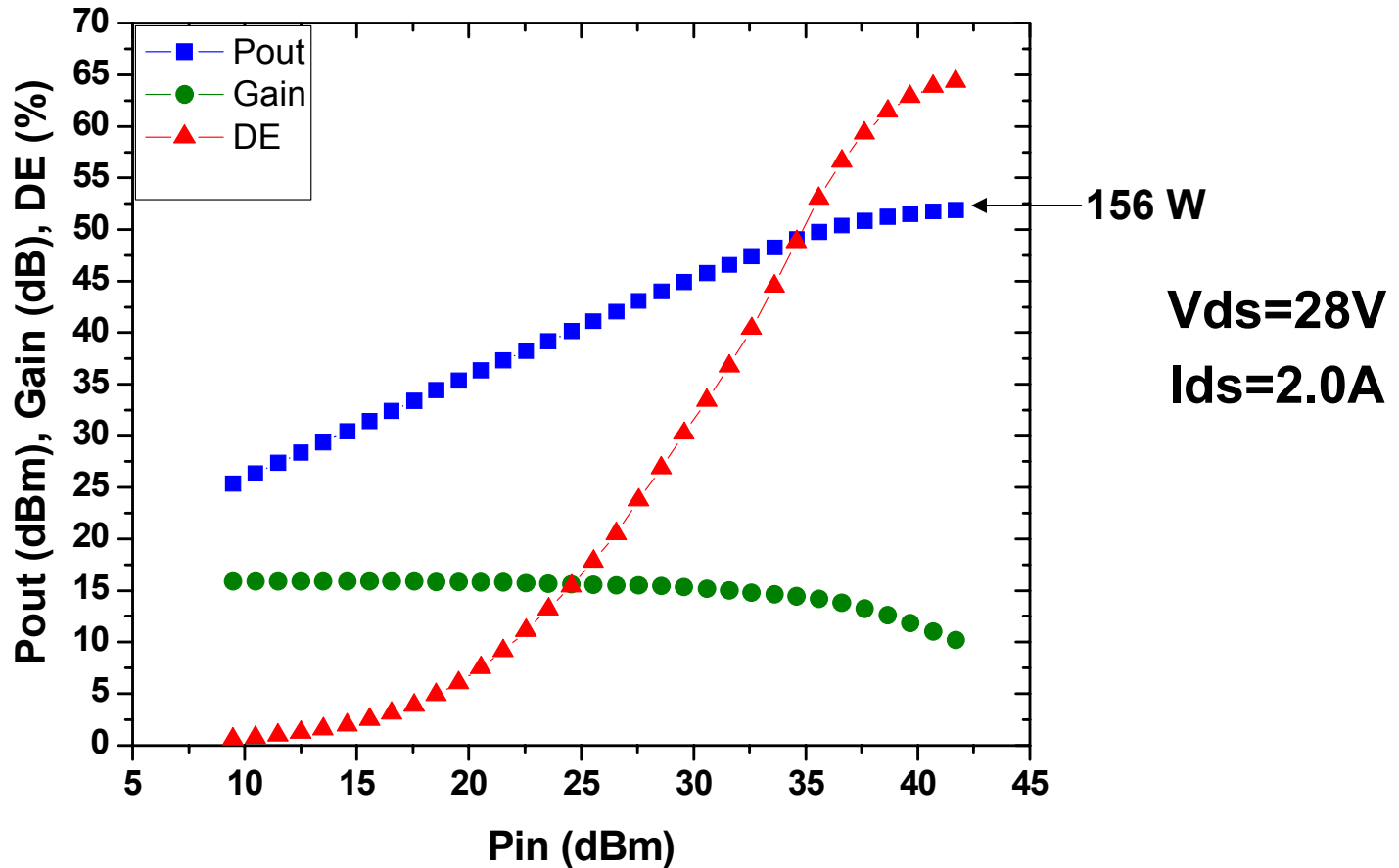


RF Test Board

CW Power Sweep

>> 156W CW power sweep at 2.14 GHz - non pulsed

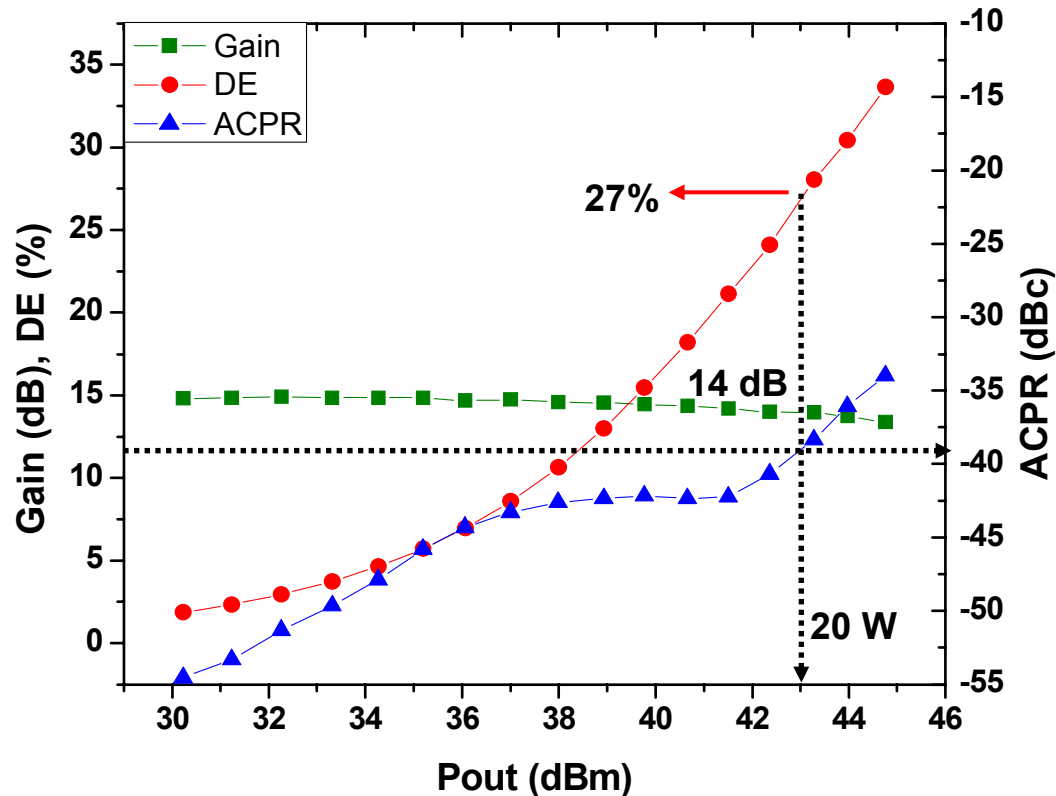
- ▶ Associated drain efficiency of 65% and small-signal gain of 16 dB



WCDMA Power Sweep

>> Application Board Results

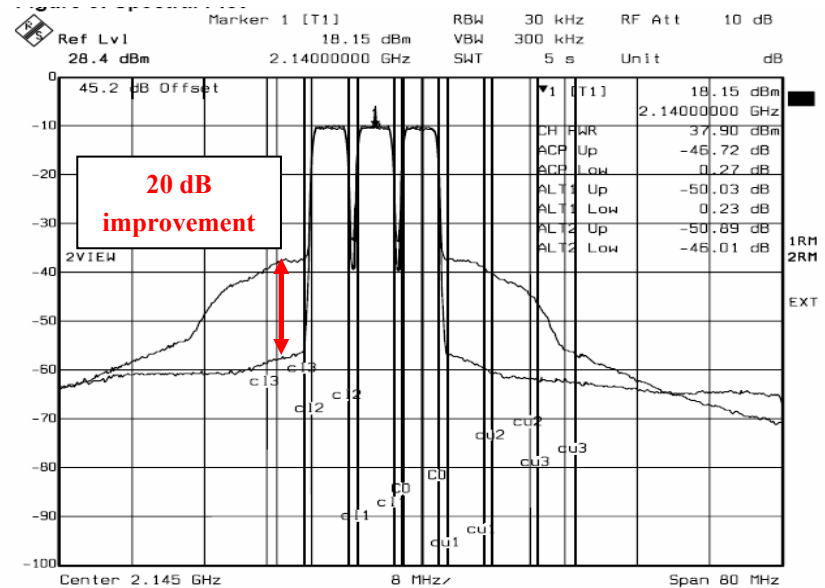
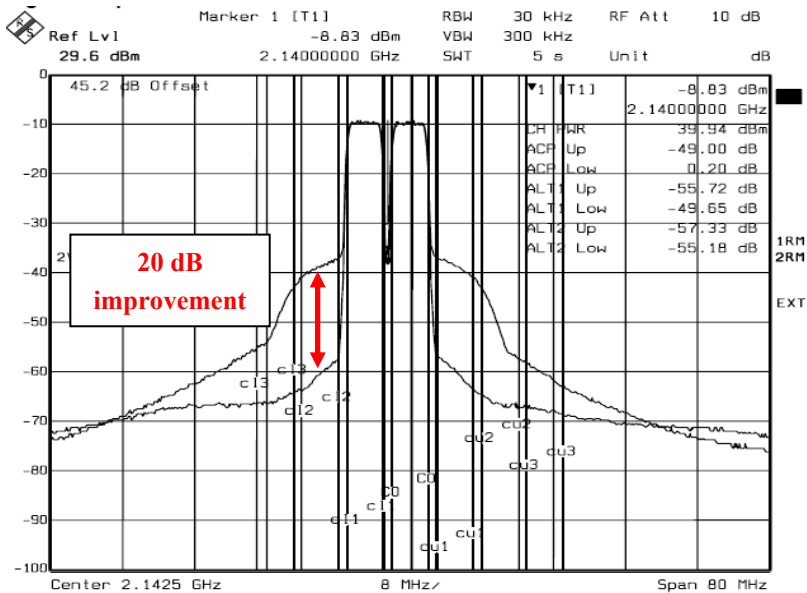
- ▶ Output power is 20 W @ -39 dBc, drain efficiency of 27% and 14 dB gain
- ▶ WCDMA 3GPP 9.8 dB PAR @ 0.01% CCDF



Vds=28V
Ids=2.0A

WCDMA DPD Results

- DPD technique was applied to a single 36 mm GaN die in a CuW ceramic package mounted to a 50 W application board.
 - ▶ The device was biased at 28 V_{dc} and 1.0 A, and was excited with two and three carrier WCDMA 3GPP compliant test signals.
 - ACPR improved by nearly 20 dB while the drain efficiency increased by ten percentage points to better than 35% yielding 19 W of RF output power.

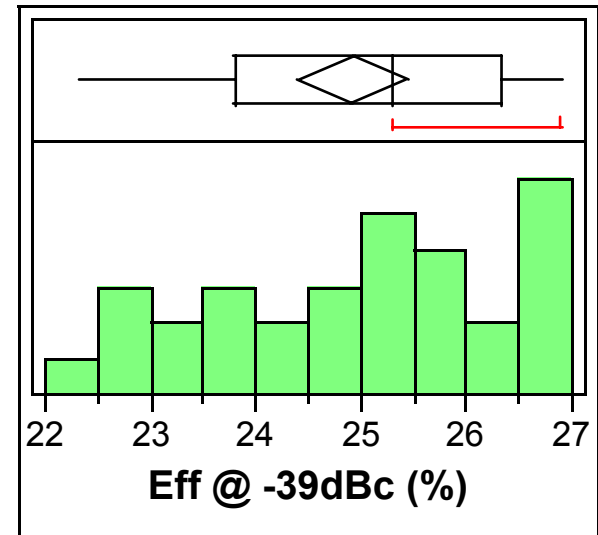
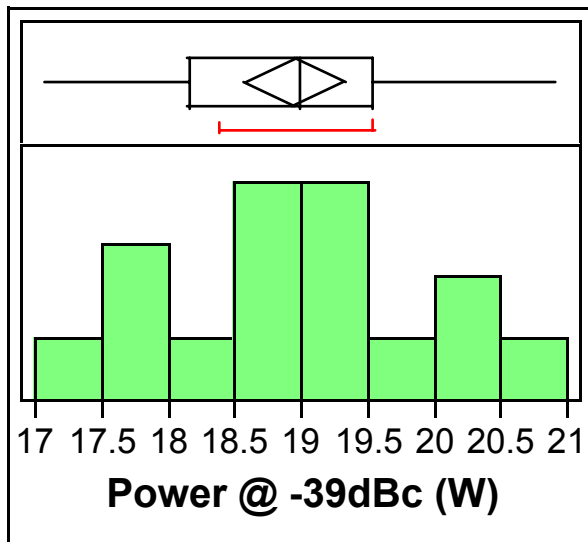


Reproducibility

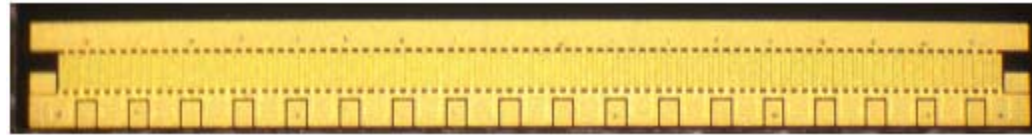
>> Histograms are from 31 devices and 3 different wafers, all from Nitronex's baseline process.

▶ Results shown @ -39dBc ACPR

- Over 25% Average DE
- Average Power of 19 W

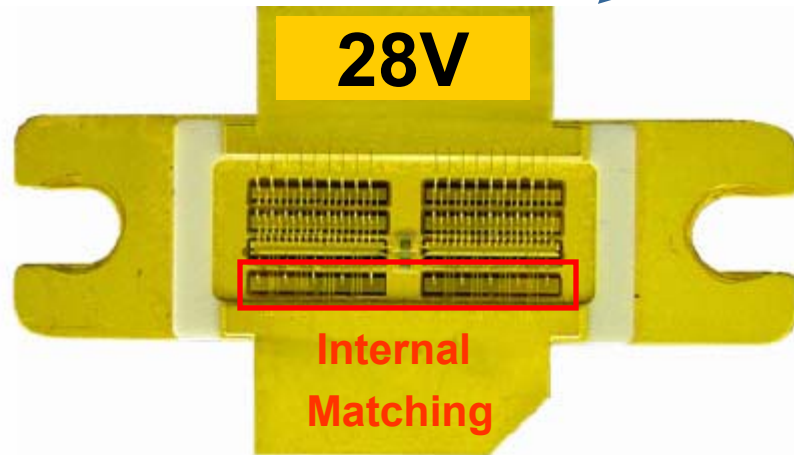


Benefits of High-Voltage



2 GaN chips

1 GaN chip



28V

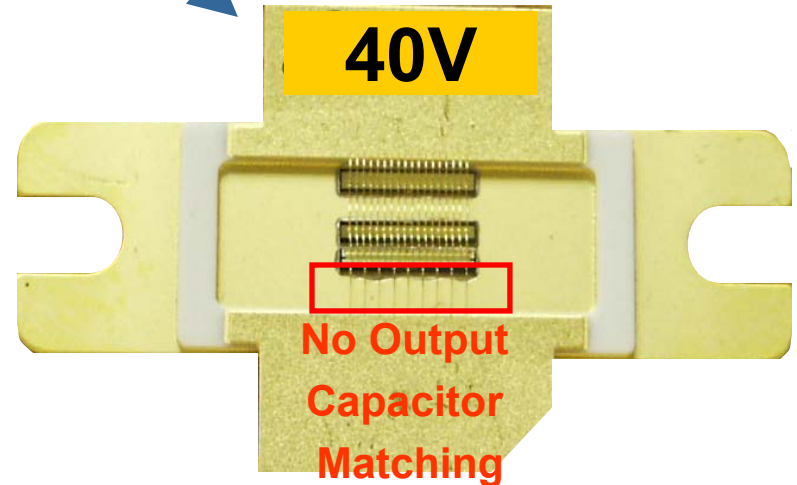
Internal
Matching

NPT21120

$Z_{out} \sim 3 \Omega$

BW = 120 MHz

$P_{sat} = 140W$ (~2W/mm)



40V

No Output
Capacitor
Matching

NPT23060

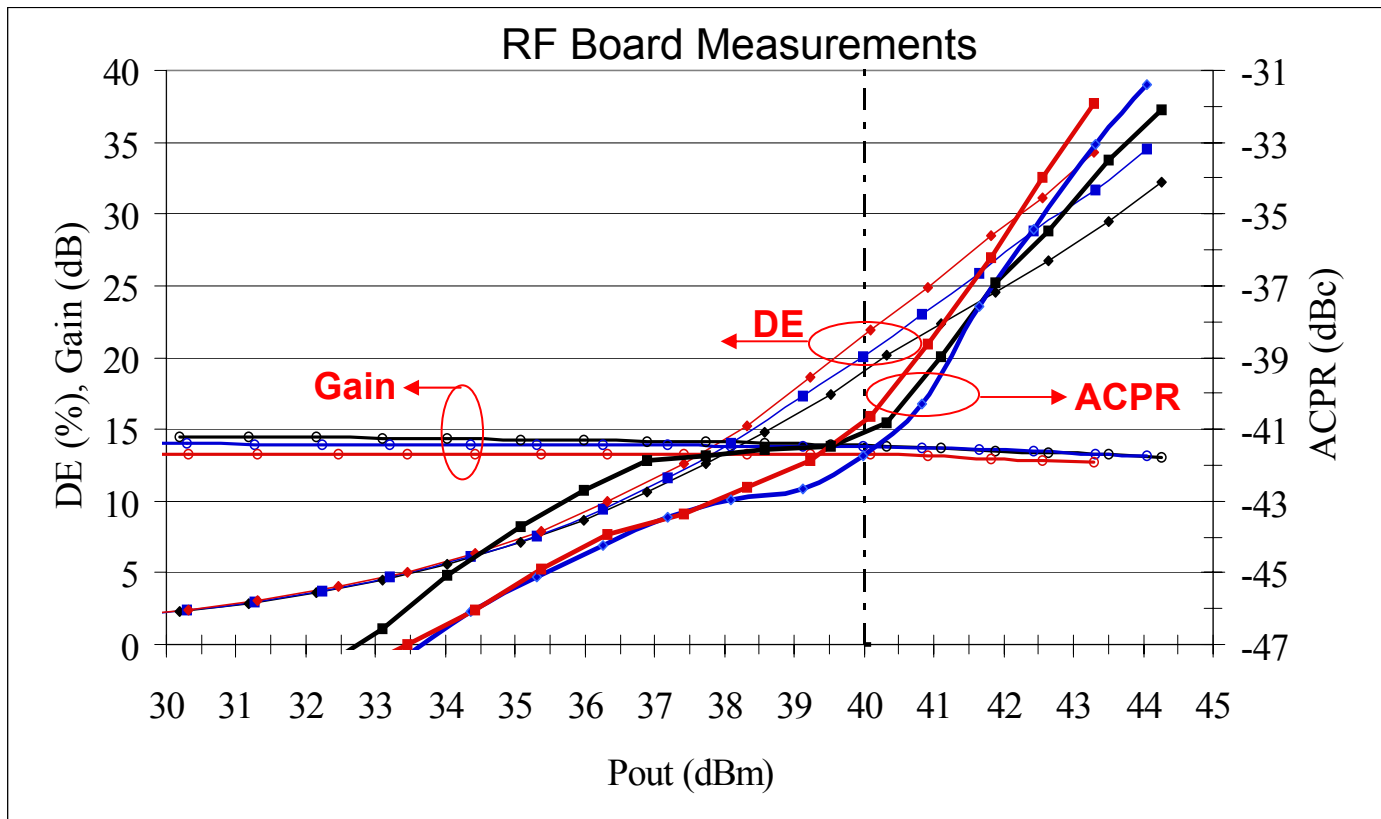
$Z_{out} \sim 7 \Omega$

BW > 300 MHz

$P_{sat} = 100W$ (~3W/mm)

Wider Bandwidth Power Devices

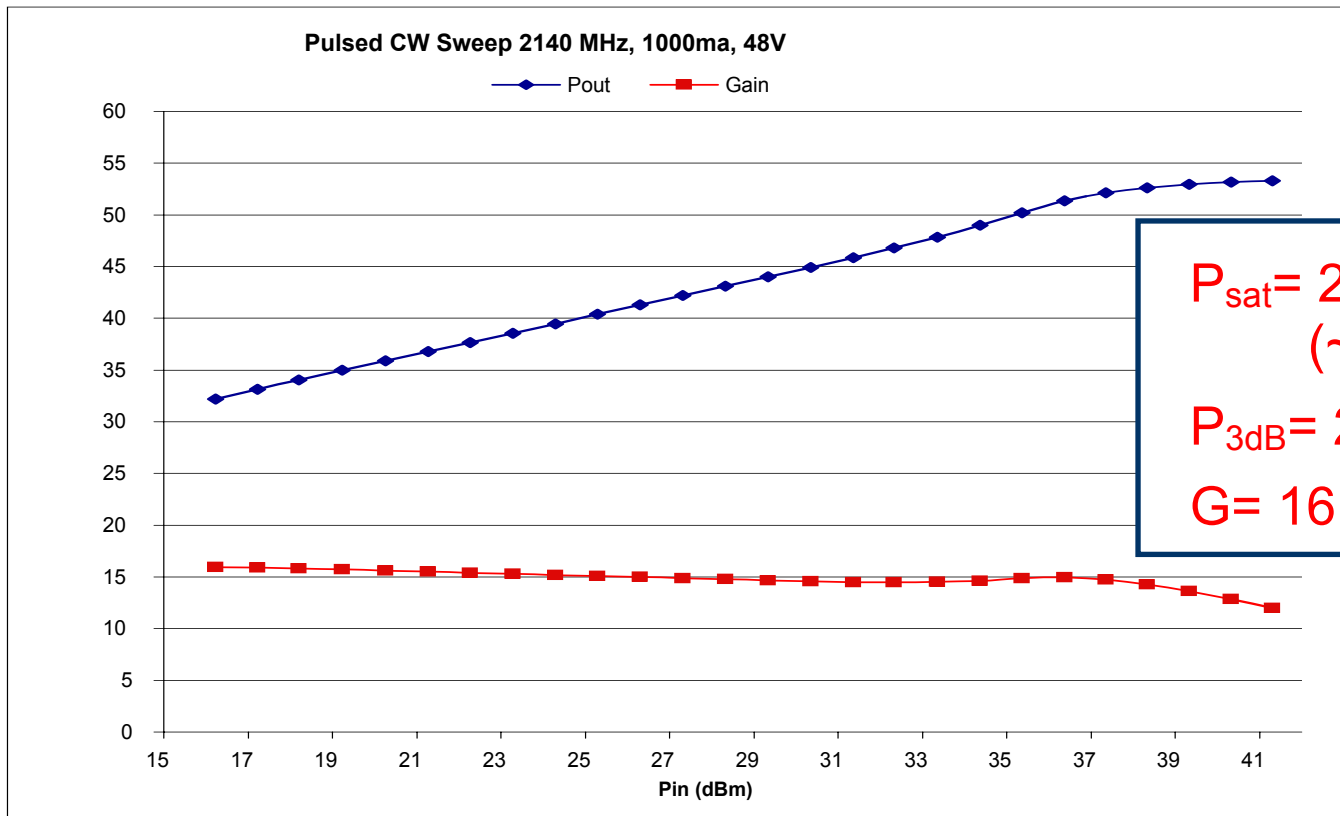
- Single 36mm die in CuW package provides over 300 MHz Bandwidth at 2.14 GHz and 40V, 1200ma
 - No internal output capacitor improves bandwidth performance



2000 MHz
2140 MHz
2280 MHz

Higher Power Levels at 48V (6W/mm)

- 48V, 1000ma, 2140 MHz, pulsed CW, 36-mm gate periphery
- Initial market applications: WCDMA broadband & Military



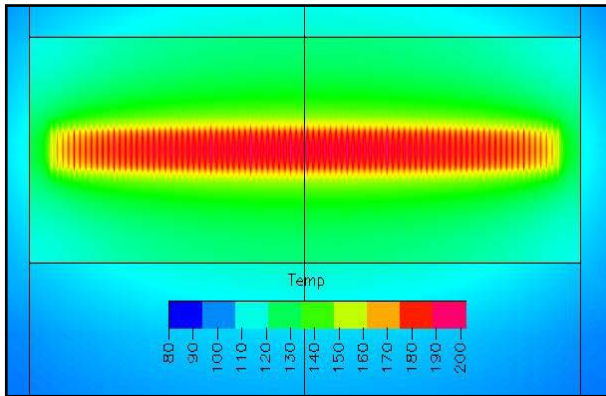
$P_{\text{sat}} = 213 \text{ W}$
(~ 6 W/mm)

$P_{3\text{dB}} = 200 \text{ W}$

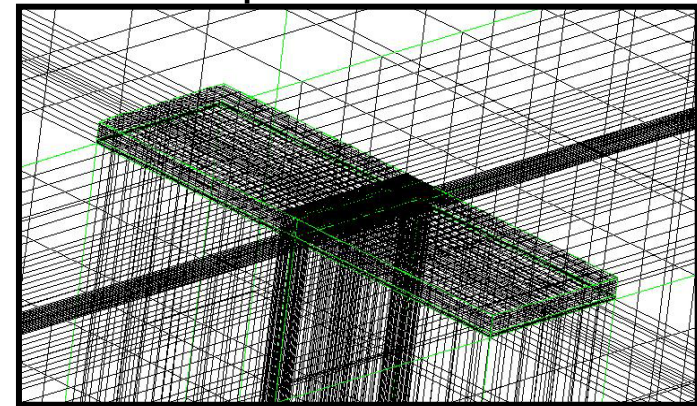
$G = 16 \text{ dB}$

Thermal Design

Finite Element Thermal Model

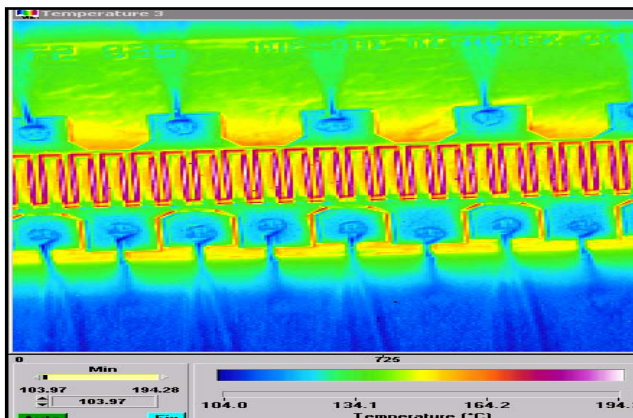


Computational Grid

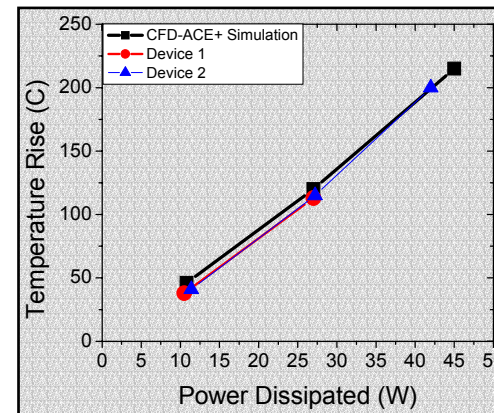


- Thermal imaging done on 90 finger cells, with 18mm in total periphery, results show very good agreement.

Thermal imaging



Model Validation





Reliability Data

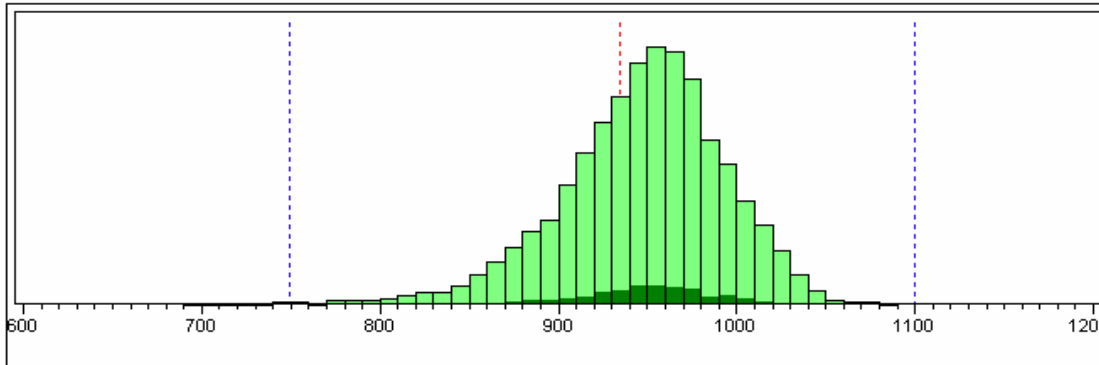
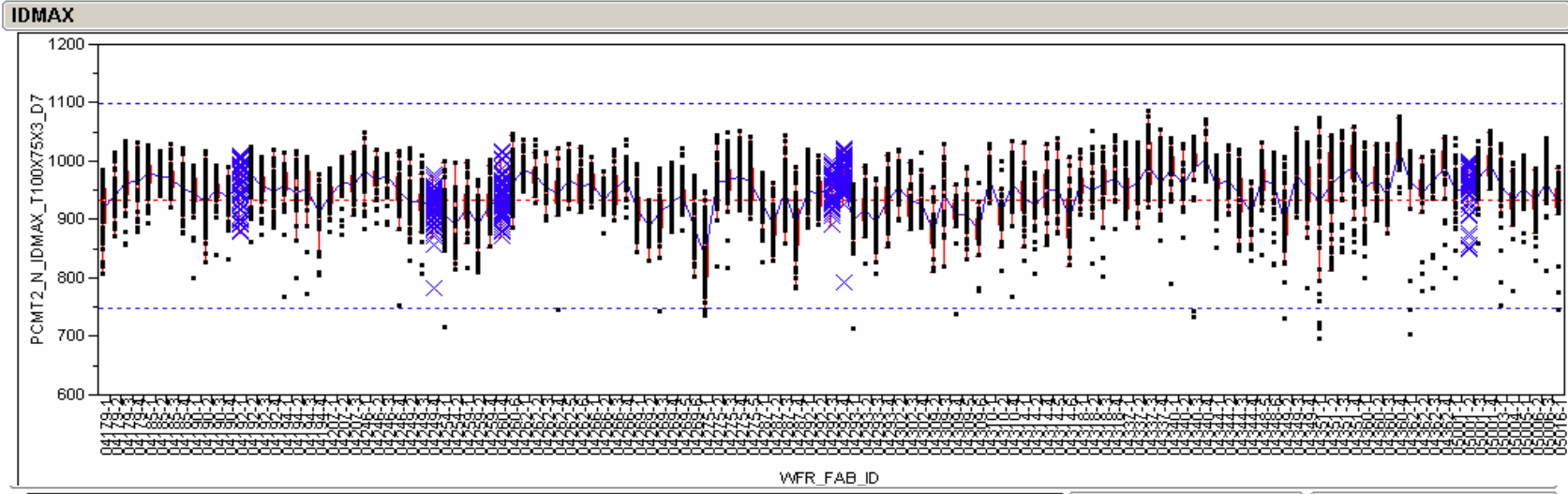
Reliability Test Plan

Chip Level Reliability Study

- On-going 24 hour burn-in stabilization
- HTOL 1000hr DC stress Stress Testing @Tj=200°C
- HTOL RF Stress Test at NSWC-Crane
- DC to RF Correlation Study
- Activation Energy Determination (3 temperature test)
- FIT and MTTF Determination
- ESD Testing
- HTRB Testing
- 5:1 VSWR
- Autoclave
- Temperature Cycling
- Failure Analysis



Baseline Control Chart (Maximum Drain Current)

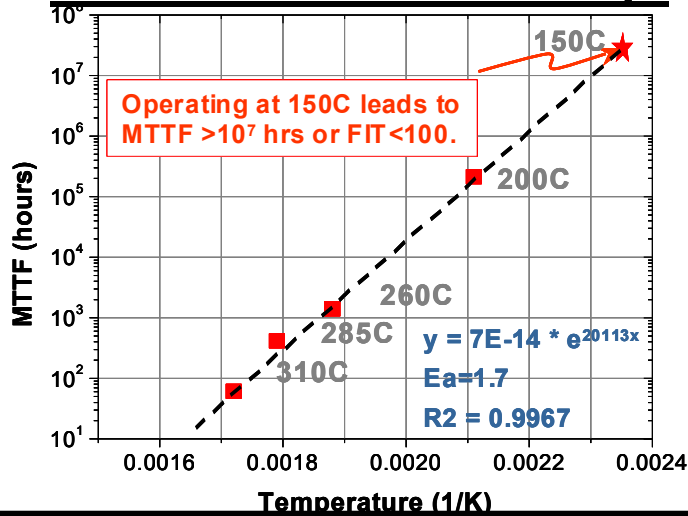


Quantiles		Moments		
100.0%	maximum	1084.3	Mean	947.01778
99.5%		1045.9	Std Dev	46.790875
97.5%		1027.7	Std Err Mean	0.5493037
90.0%		1002.9	upper 95% Mean	948.09457
75.0%	quartile	977.7	lower 95% Mean	945.94098
50.0%	median	951.4	N	7256
25.0%	quartile	920.6		
10.0%		887.8		
2.5%		843.9		
0.5%		777.0		
0.0%	minimum	694.0		

- Control chart for Idmax across 150 baseline wafers over past 1 year.
 - ▶ Data taken on 100 μ m PCM structure. All reticles on wafer tested.
- Wafers used in reliability testing highlighted in blue (6 wafers, 5 lots).

Reliability Status

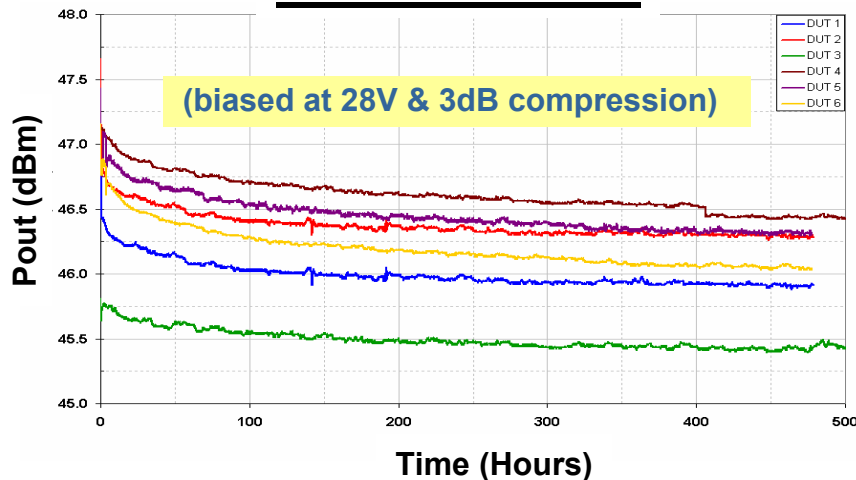
Drift vs. Time and Temp.



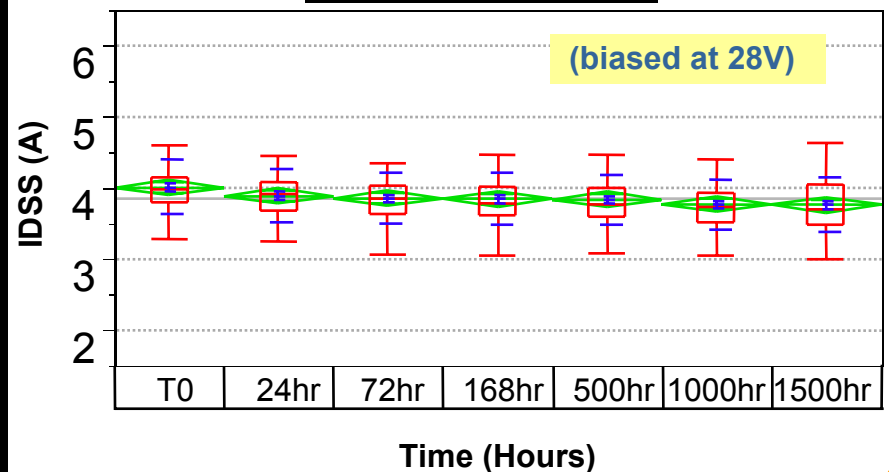
Reliability Summary

- **3-Temp Stress:**
 - Activation energy 1.7eV
 - MTTF >10⁷ at 150°C
 - FIT <100
- **RF-Stress:** P_{sat} drift over 20 years at 200°C is <1dB
- **HTOL:** I_{dss} drift over 20 years at 200°C is <15% (150C is <6%)

RF Stress Plot



DC HTOL Plot



Summary

- GaN on Si has demonstrated high power levels and high performance
 - ▶ Current baseline supports 28V operation
- Higher voltage operation leads to broader bandwidth and higher power densities for large periphery devices
- Broadband RF power transistors are being developed to support commercial and military applications
- Repeatable high performing baseline demonstrated
 - ▶ Large periphery results consistently >2W/mm and 60% efficiency.
- Reliability data shows promising initial results
 - ▶ 3-temp data shows expected exponential relationship between drift and temperature (activation energy ~ 1.7eV).
 - ▶ HTOL data shows 20 yr. drift <15% in all parameters at stress temperature of 200°C and ~6% drift at use temperature of 150°C.
 - ▶ RF Stress data shows 20 yr. drift <1dB and similar trends to DC.
 - ▶ ESD data is equivalent to or better than existing technologies without any protection circuitry.