NITRONEX
CORPORATION

NPT35050A Qualification Document

Revision 2

NITRONEX CORPORATION

NPT35050A Qualification Document

Qualification Document for NPT35050 Product

1.0 Purpose

This document outlines the qualification of the NPT35050A device.

2.0 Customers and/or Applications

RF products for use in wireless communications infrastructure.

3.0 NRF1 Technology Definition

3.1 Technology Features

The Nitronex NRF1 technology was designed to support product development for linear and broadband applications to 3.8GHz with operational voltage of 28V.

Key features of NRF1 technology include:

- High-resistivity (>10k Ohm-cm) silicon substrate
- Ti/Al/Ni/Au ohmic contacts
- 0.5µm Ni/Au T-gate electrode
- SiN_x passivation and encapsulation layers
- Electroplated gold air-bridge interconnect level
- Through-substrate ground vias
- 150µm final substrate thickness

Mask count consists of 10 photo levels, 9 reticles and 1 contact plate. An optional label feature introduces an additional contact plate to the count.

3.2 Process Performance Results

- Psat > 3.5W/mm with Drain Efficiency > 60% at 2.14GHz and 28V
- Maximum Drain current > 800mA/mm
- Contact Resistance < 0.5 Ω-mm
- Breakdown Voltage > 100V
- Maximum Drain Current drift of less than 5% over 20 years at T_J=150°C, V_{DS}=28V

3.3 In-line Process Data

NRF1 process platform was released in October 2005. Specification limits have been established for inline performance under both DC and RF stimulus. A list of the parameters and limits is given in Table 1 below. To date over 200 wafers have been run through this process flow with high yield.

Table 1: Specification limits for DC and RF inline tests.

Parameter	Description	Units	LSL	TGT	USL
BVDG	Two Terminal Off-State Breakdown Voltage	V	135	160	-
BVDS	Three Terminal Off-State Breakdown Voltage	V	95	130	-
GMX	Maximum Extrinsic Transconductance	mS/mm	250	290	330
IDLK_100	Drain Leakage	mA/mm	-	0.2	1.0
IDMAX	Maximum Open Channel Current	mA/mm	760	830	900
LOG_ISO	Isolation Leakage Current - LOG10	Log(A)	-	-9	-8
RC_TLM	Contact Resistance	Ohm mm	-	0.38	0.55
RDON	On Resistance	Ohm mm	2.4	3.0	3.6
RSH_CRBME	Epitaxial Layer Sheet Resistance	Ohm/sq	440	490	530
VP	Pinchoff Voltage	V	-1.50	-1.25	-1.00
NPSAT_W_MM	Saturated Output Power	W/mm	3.4	3.9	-
DEFF_MAX	Maximum Drain Efficiency	%	57	62.5	-

4.0 NPT35050A Device Definition

4.1 Device Features

The NPT35050A consists of a single 36mm die (0.75mm x 5.65mm chip dimensions) and two input capacitor die with a AuSi eutectic bond to a CPC (Cu/CuMo laminate) ceramic package with ceramic lid attached via an epoxy seal (non-hermetic) forming an open cavity body. The 36mm die is formed by putting multiple 2mm unit cell devices in parallel. Figure 1 below show layout pictures of the 2mm building block device and the 36mm product die.

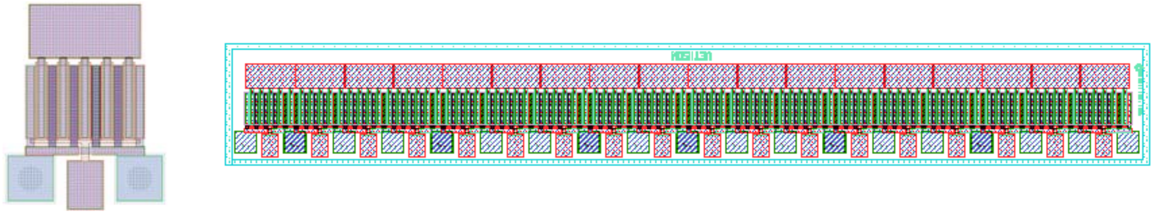

Figure 1: Layout drawings of 2mm building block (left) and 36mm product die (right)

Figure 2 shows a picture of the packaged NPT35050A product device.

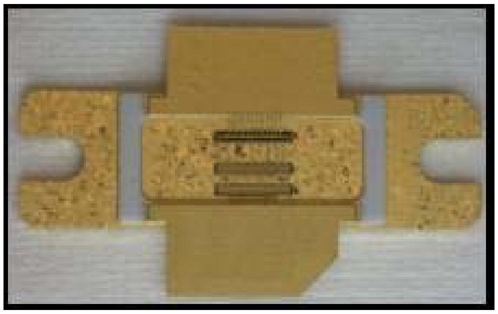

Figure 2: Picture of the NPT35050A.

4.2 Device Performance Results

- OFDM Performance at V_{DS}=28V and P_{out}=6W from 3.3-3.8GHz:
  - EVM < 2.5%
  - Gain > 10dB
  - Drain Eff. > 18%
- CW Saturated performance of greater than 65W and 45% at 3.5GHz and 28V.

4.3 Final Device Data

A battery of RF tests was performed on a nominal set of devices to obtain typical characteristics for the NPT35050A product. Multiple devices from 3 process lots were put through CW, Pulsed, 2-tone PEP, EVM, and temperature dependent testing. Results are as follows.

4.3.1 CW, Pulsed, and PEP Performance

CW, pulsed (100µs pulse width, 1% duty cycle), and 2-tone PEP (100khz spacing) were taken on all samples with V_{DS}=28V, I_{DQ}=750mA, and Frequency=3.5GHz. A typical CW plot and a comparison of CW, pulsed, and PEP power is shown in Fig. 3.

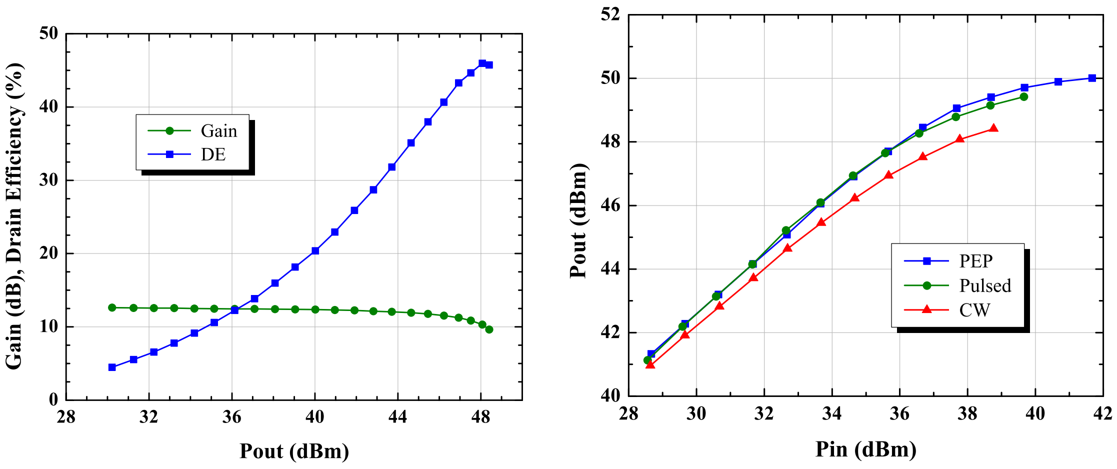

Figure 3: CW power sweep at 3.5GHz (left) and comparison of CW, Pulsed, and PEP power (right).

4.3.2 OFDM Performance

OFDM performance is measured over the frequency range of 3.3GHz to 3.8GHz with a single carrier OFDM waveform (64-QAM ¾, 8 burst, 3.5MHz channel bandwidth, 10.3dB PAR @ 0.01% probability). All measurements are taken with a bias point of V_{DS}=28V and I_{DQ}=750mA.

Figure 4 shows the EVM performance versus frequency and a plot of EVM performance versus power for 3.4 and 3.6GHz.

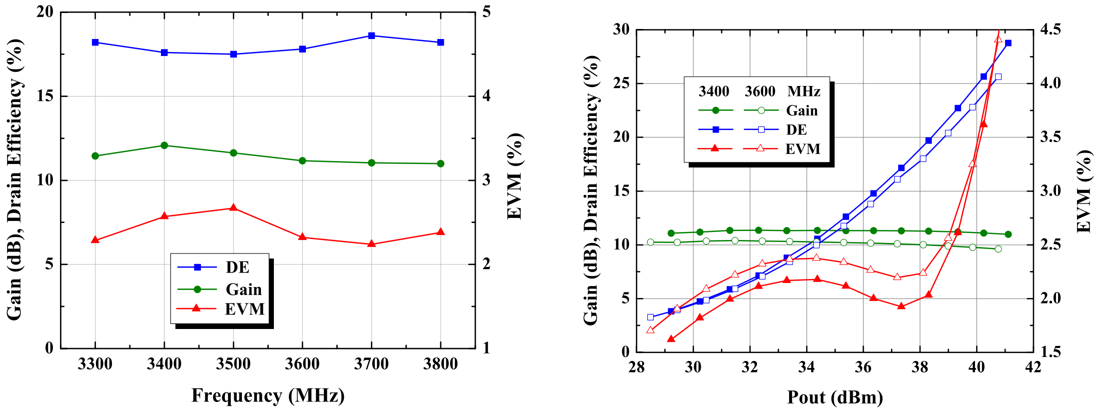

Figure 4: OFDM performance vs frequency at P_{out}=38dBm (left) and EVM curves at 3.4 and 3.6GHz (right).

4.3.3 Temperature Dependent Behavior

In order to study the effects of temperature, OFDM measurements were made at multiple case temperatures of -40, -20, 0, 20, 40, 60, and 85°C. Figure 5 shows OFDM power sweeps at multiple temperatures and demonstrates consistent behavior across the temperature range of interest.

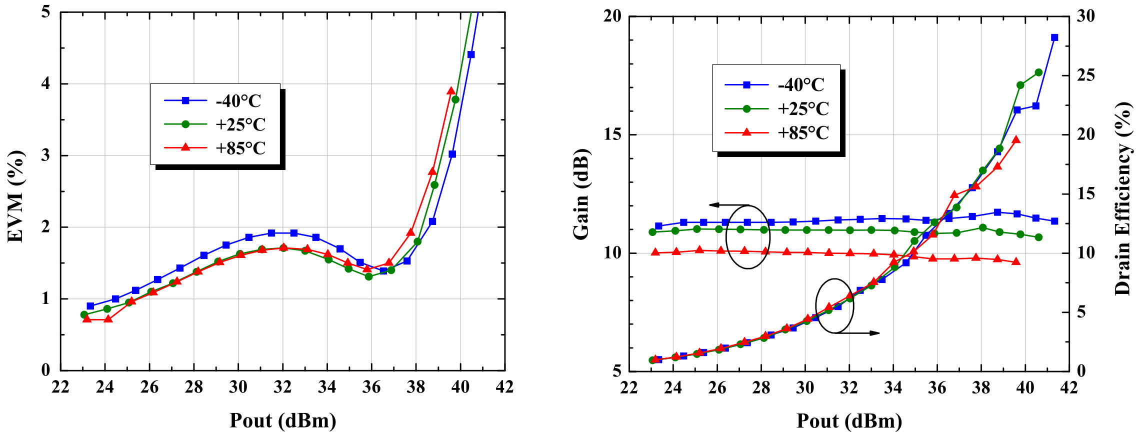

Figure 5: OFDM performance as a function of temperature; EVM (left), Gain and Efficiency (right)

5.0 Qualification Data

Section 5 presents the qualification data for the NPT35050A product. The first section details the plan approved by the Technology Qualification Review Board (TQRB) on September 15, 2005. The second section contains results from all the reliability tests.

5.1 Reliability plan

Qualification is divided into 4 blocks:

- Product Device Tests
- Product Assembly Tests
- Other packaged tests
- Intrinsic Device Tests

The flow chart in Fig. 6 below details which tests are included in each block.

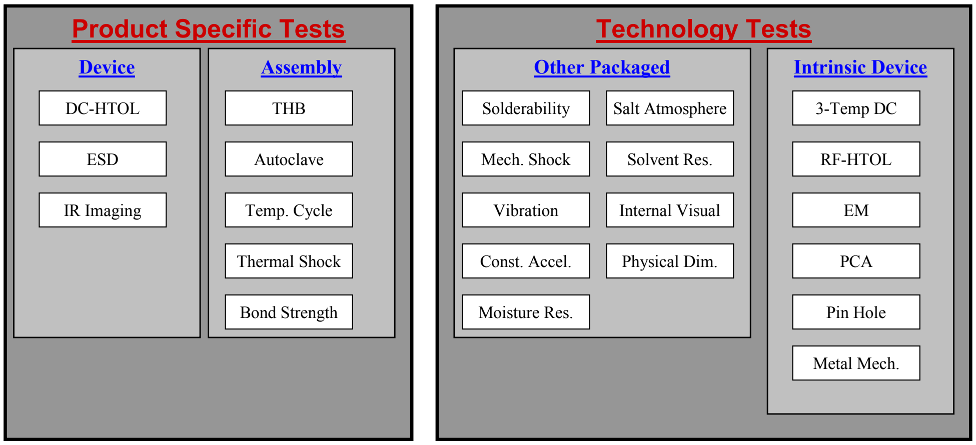

Figure 6: Flow chart detailing different test blocks and specific tests.

5.1.1 Sample Sizes

A minimum of 3 lots will be used in all samples sets. The number of samples and allowed failures are based on LTPD statistics (90% confidence) and are given in the test descriptions that follow.

5.1.2 Device Burn-In

Devices will go through a burn-in prior to commencement of life-test.

5.1.3 DC Test Conditions

DC testing will be performed before and after stress to determine device degradation. Table 2 summarizes DC data taken during down-point measurements.

Table 2: DC Measurement List

Parameter	Description	Units
Idmax	Maximum Drain Current (I_{GS}=+36mA, V_{DS} =7V, pulsed)	A
Vp	Pinch-off Voltage (I_{DS}=36mA, V_{DS}=28V)	V
IDLK60	60V Drain Leakage (V_{GS} =-8V, V_{DS} =60V)	mA
Rdon	On-Resistance (V_{GS}=0V, I_{DS} =180mA and I_{DS} =360mA	Ω

5.1.4 RF Test Conditions

RF testing will be performed before and after stress to determine device degradation. RF testing will consist of power sweeps under OFDM modulation at V_{ds}=28V, Freq=3.4 and 3.6GHz, and T_F=25°C in a 50-ohm application board. Table 3 summarizes RF data taken during down-point measurements.

Table 3: RF Measurement List

Parameter	Description	Units
Idq	Quiescent drain current measured at fixed Vg.	A
EVM @ P_{out} = 38dBm	EVM measured at a Pout level of 38dBm	%
Gain @ P_{out} = 38dBm	Gain measured at a Pout level of 38dBm	dB
DE @ P_{out} = 38dBm	Drain Efficiency measured at a Pout level of 38dBm	%

5.1.5 Pass/Fail Criteria

Soft Failures – 15% drift in DC on-state parameters, 10x increase in leakage parameters, or 1dB drift in RF parameters.

Hard Failure – Catastrophic device failure.

5.1.6 Product Device Level Tests

5.1.6.1 DC High Temperature Operating Life (DC-HTOL)

Testing will be performed under DC stress at V_{DS}=28V and T_J=200°C for 1000 hours in accordance with JESD22A108A. Intermediate testing will be performed at 48, 168, and 500 hours, with a final readout at 1000 hours. All testing will consist of a full DC and RF characterization suite according to Tables 2 and 3.

Sample Size: To reach an LTPD level of 5, requires either 45 samples with 0 failures or 77 samples with 1 failure. Samples will be taken randomly from a minimum of 3 processed lots.

5.1.6.2 Electrostatic Discharge – Human Body Model (ESD-HBM)

Three devices per voltage per wafer will be stressed according to 1020/Mil-Std-750. Voltages of 500V, 1000V, 2000V, and 4000V will be attempted. For each voltage all pin combination will be stressed with 3 ESD pulses. The ESD-HBM threshold will be the highest passing voltage.

5.1.6.3 Electrostatic Discharge - Machine Model (ESD-MM)

Three devices per voltage per wafer will be stressed according to 1020/Mil-Std-750. Voltages of 50V, 100V, 200V, and 400V will be attempted. For each voltage all pin combination will be stressed with 3 ESD pulses. The ESD-MM threshold will be the highest passing voltage.

5.1.6.4 Thermal Impedance

Thermal impedance will be characterized on a minimum of 5 samples using IR microscopy under a baseplate temperature of 80°C. Whenever possible thermal impedance test conditions will mimic actual fixturing and bias conditions used during life test.

5.1.6.5 VSWR Testing

Output of device is terminated with 10:1 mismatch and line stretcher used to rotate mismatch through all angles. Device is held at operating output power during stress.

5.1.7 Product Assembly Level Tests

5.1.7.1 Autoclave

Autoclave testing will be carried out at 121°C, 100%RH, and 15psi for 96 hours per JESD22A108A. Electrical testing will be carried out before and after the stress according to Tables 2 and 3. 125°C, 24hr bake allowed prior to final electrical test.

Sample Size: To reach an LTPD level of 5, requires either 45 samples with 0 failures or 77 samples with 1 failure. Samples will be taken randomly from 3 process lots.

5.1.7.2 Temperature Cycle

Temperature Cycling will consist of air-to-air cycling between –65°C and 150°C per Mil-Std-750. There will be a total of 500 cycles with electrical testing before and after the stress according to Tables 2 and 3.

Sample Size: To reach an LTPD level of 5, requires either 45 samples with 0 failures or 77 samples with 1 failure. Samples will be taken randomly from a minimum of 3 process lots.

5.1.7.3 Temperature Shock

Temperature Shock will consist of liquid-to-liquid cycling between –55°C and 125°C per Mil-Std-750. There will be a total of 100 cycles with electrical testing before and after the stress according to Tables 2 and 3.

Sample Size: To reach an LTPD level of 15, requires 15 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.7.4 Bond Strength

Bond Strength will be tested per Mil-Std-750-2037.

Sample Size: To reach an LTPD level of 15, requires 15 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.8 Other Packaged Tests

5.1.8.1 Solderability

Solderability tested per JESD22-B102 at 245°C using mechanical samples.

Sample Size: 4 devices per lot.

5.1.8.2 Mechanical Shock

Mechanical Shock will be tested per Mil-Std-833-2002 at 1500g's.

Sample Size: To reach an LTPD level of 10, requires 38 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.8.3 Vibration

Vibration testing performed per Mil-Std-833-2007 from 20Hz to 2000KHz with a peak force of 20g.

Sample Size: To reach an LTPD level of 10, requires 38 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.8.4 Constant Acceleration

Constant Acceleration will be performed per Mil-Std-833-2001 at 10,000g's.

Sample Size: To reach an LTPD level of 10, requires 38 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.8.5 Solvent Resistance

Solvent Resistance will be test per M-833-2015.

Sample Size: To reach an LTPD level of 15, requires 15 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.8.6 Salt Atmosphere

This test shall be performed per Mil-Std-833-1009 for 24 hours. The failure criteria for this test is visual inspection and this is considered a destructive test.

Sample Size: To reach an LTPD level of 15, requires 15 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.8.7 Moisture Resistance

Moisture Resistance will be test per Mil-Std-833-1004. The failure criteria for this test is visual inspection and this is considered a destructive test.

Sample Size: To reach an LTPD level of 10, requires 38 samples with 0 failures. Samples will be taken randomly from a minimum of 3 process lots.

5.1.9 Intrinsic Device Tests

5.1.9.1 3-Temp DC Life Test

Testing will be performed on a minimum of 2 wafers from 3 lots. Stressing will be carried out at DC quiescent conditions and elevated temperatures between 200°C and 350°C. The lowest temperature will be stressed for 1000-2000 hours while the highest temperature will be stressed for 100-500 hours. In-situ drain current monitoring will be used to determine failures with a 15% drift criteria. Data will be used to determine activation energy and FIT rate. The MTTF should be greater than 10^6 hours at 150°C junction temperature.

5.1.9.2 RF High Temperature Operating Life (RF-HTOL)

Testing will be performed on a minimum of 2 wafers from 3 lots. Stressing will be carried out at DC quiescent conditions with RF applied at 3-dB compression level and T_J=200°C. In-situ Pout monitoring will be used to determine failures with a 1dB drift criteria. Data will be correlated with DC-HTOL testing and ensure same failure modes apply with DC and RF.

5.2 Reliability Results

Reliability testing was performed according to the plan in section 5.1 and results of all tests are summarized in Table 4 below. Details of individual tests are shown in the following sections.

Table 4: Summary of Reliability Test Data

Test Name	Test Standard	Sample Set	Status
3-Temp DC	JEP118-B	30 Devices/Temp @ 260, 285, and 310°C	**Complete**
DC-HTOL	JESD22-A108	45 devices, 1000 hours	**Complete**
RF-HTOL	JESD22-A101-A	6 Devices, 500 hours	**Complete**
ESD-HBM	M-750-1020	9	**Complete**
ESD-MM	M-750-1020	9	**Complete**
Thermal Impedance	IR imaging	9	**Complete**
Autoclave	JESD22-A102	45	**Passed**
VSWR	10:1 VSWR	5	**Passed**
Temp. Cycling	JESD22-A104	45	**Passed**
Thermal Shock	M-750-1056	15	**Passed**
Solderability	JESD22-B102	4	**Passed**
Mech. Shock	M-883-2002	38	**Passed**
Vibration	M-883-2007	38	**Passed**
Const. Acceleration	M-883-2001	38	**Passed**
Moisture Res.	M-883-1004	38	**Passed**
Salt Atmosphere	M-883-1009	15	**Passed**
Solvent Res.	M-833-2015	15	**Passed**
Bond Strength	M-750-2037	15	**Passed**

5.2.1 3-Temperature DC Results

3-Temperature DC testing was carried out in order to determine the activation energy for the NRF1 process. Testing consisted of DC stress at V_{DS}=28V and I_{DS}=2.34A with ambient temperature adjusted to achieve junction temperatures of 260°C, 285°, and 310°C. For each stress temperature 25-30 devices were tested with stress time ranging from 400 to 1000 hours. A failure criteria of 15% drift in in-situ drain current was used. Failures followed a lognormal distribution and cumulative failure plots were used to asses the MTTF for each temperature group. An Arrhenius plot of activation energy is shown in Fig. 7 below.

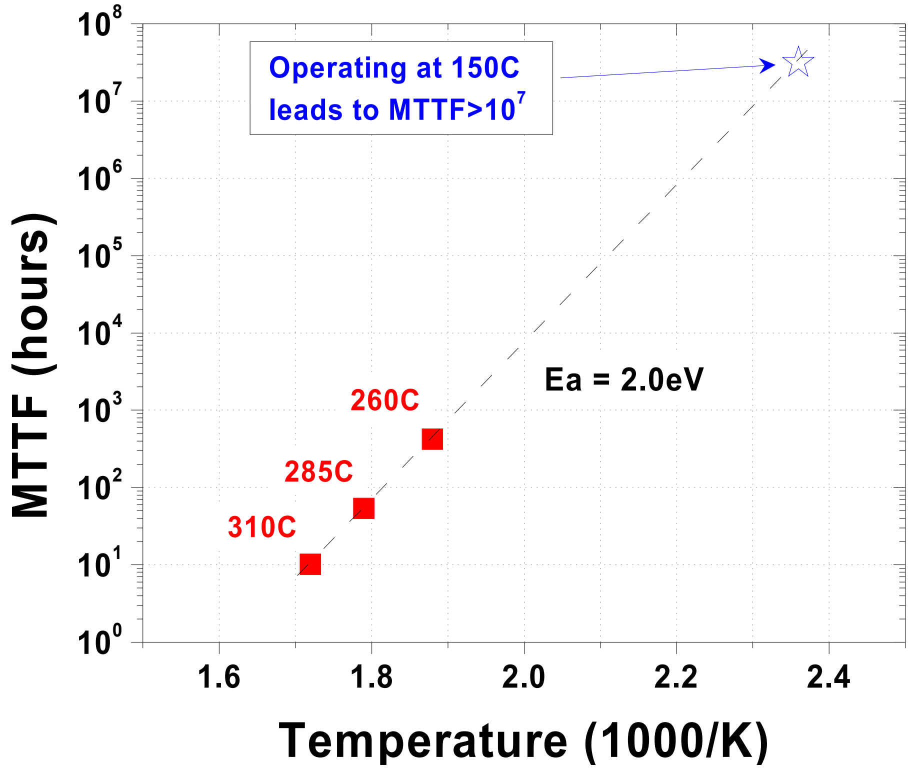

Figure 7: Arrhenius plot showing Activation Energy of 2.0eV and MTTF > 10^7 hours at 150°C.

From this figure it can be seen that the activation energy is 2.0eV and extrapolating to a typical use temperature of 150°C leads to a MTTF greater than 10^7 hours.

5.2.2 DC-HTOL Results

A 45 piece sample was placed under DC-HTOL stress for 1000 hours and results are shown in Fig. 8 below for maximum drain current and gain. The box plots show consistent performance between the 45 samples and minimal drift with time. Figure 9 is used to predict the long term drift rate. In this figure each of the red dots represents the median for the 45 samples at the test downpoints of 0, 36, 168, 500, and 1000 hours. The data is fit to a logarithmic relationship versus time and extrapolated forward to 20-years of operation showing a drift of <7% in maximum drain current under 200°C operation. The previously determined activation energy of 2.0eV can be used to calculated an acceleration factor and predict the drift at a more typical operating temperature of 150°C. This 150°C drift is seen in the blue curve and shows <3% drift over 20 years.

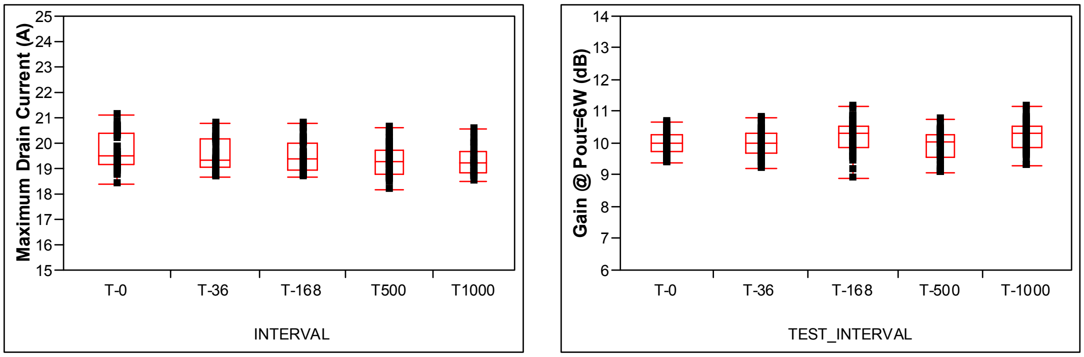

Figure 8: DC-HTOL results for maximum drain current (left) and Gain (right).

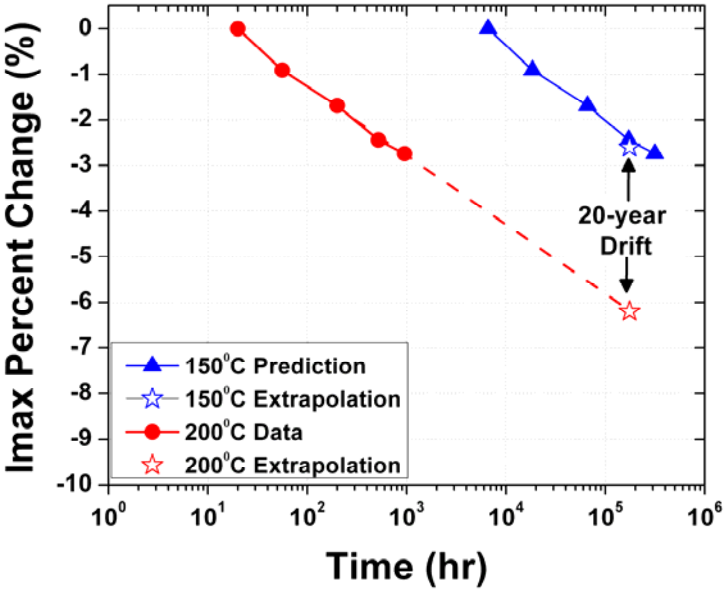

Figure 9: DC-HTOL results measured at 200°C (red) and converted to 150°C (blue) showing drift out to 20-years.

5.2.3 RF-HTOL Results

RF-HTOL testing was carried out in order to verify that the addition of RF stimulus did not create any additional failure mechanisms. A total of 6 samples were stressed at V_{DS}=28V, Freq=2.14GHz, and P_{in} sufficient to drive the device into 3dB gain compression with the baseplate adjusted to produce a T_J=200°C. Fig. 10 shows the drift in the in-situ P_{out} versus time for the 6 samples. There were two test issues which lead to systematic shifts in the data. The first issue occurred around 130 hours and was a drift in the input amplifier causing the P_{in} delivered to the devices to drop ~0.25dB. The second issue occurred at 388 hours and involved a chiller failure which caused the junction temperature to rise significantly before the devices were powered down. Some devices experienced junction temperatures as high as 400°C for 10-20 minutes. After resetting the junction temperature all devices came back to within 0.2dB of original value except DUT 6 which lost about 0.5dB in performance.

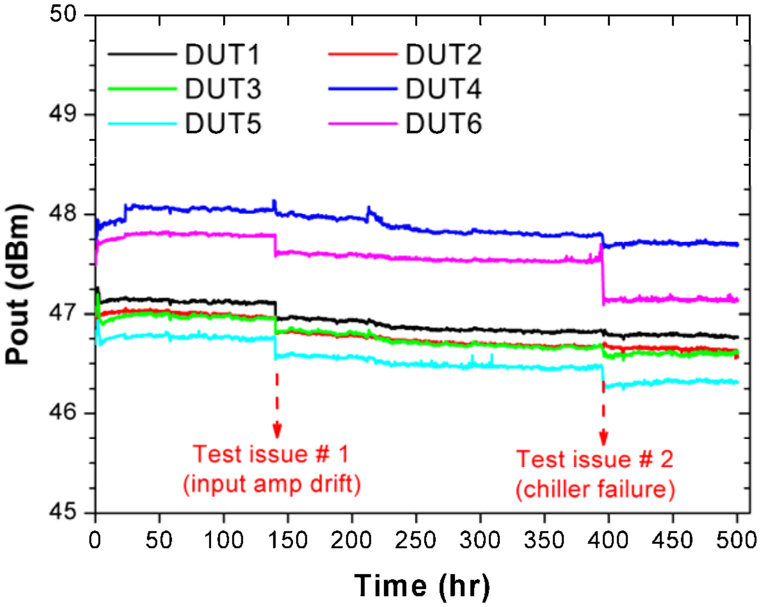

Figure 10: RF-HTOL results on 6 samples at V_{ds}=28V, P_{out}~47dBm, and T_j=200°C.

5.2.4 ESD-HBM Results

ESD testing was carried out using the HBM waveform on 3 devices each from 3 different wafers. Each pin combination (-GS, +GS, -GD, +GD) was stressed with 3 test pulses and full DC characterization was performed before and after stress. Figure 11 shows results after a HBM voltage stress of 500V and 1000V. No damage was seen after 1000V, leading to a classification of 1C.

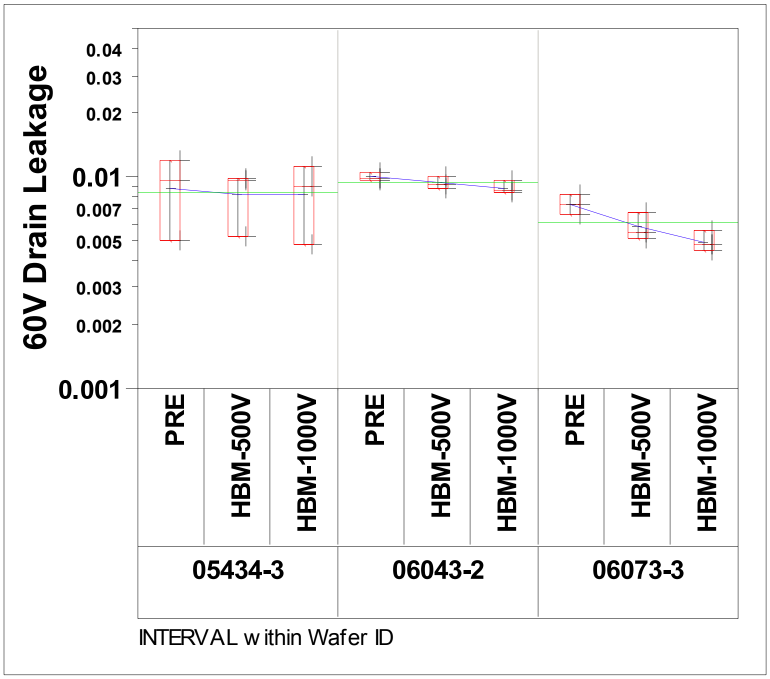

Figure 11: 60V Drain leakage shown on 3 wafers before stress and after stimulus with HBM voltages of 500V and 1000V. No failures or significant shifts in performance.

5.2.5 ESD-MM Results

ESD testing was also carried out using the MM waveform on 3 devices each from 3 different wafers. Each pin combination (-GS, +GS, -GD, +GD) was stressed with 3 test pulses and full DC characterization was performed before and after stress. Figure 12 shows results after a HBM voltage stress of 100V and 200V. No damage was seen after 200V, leading to a classification of M3.

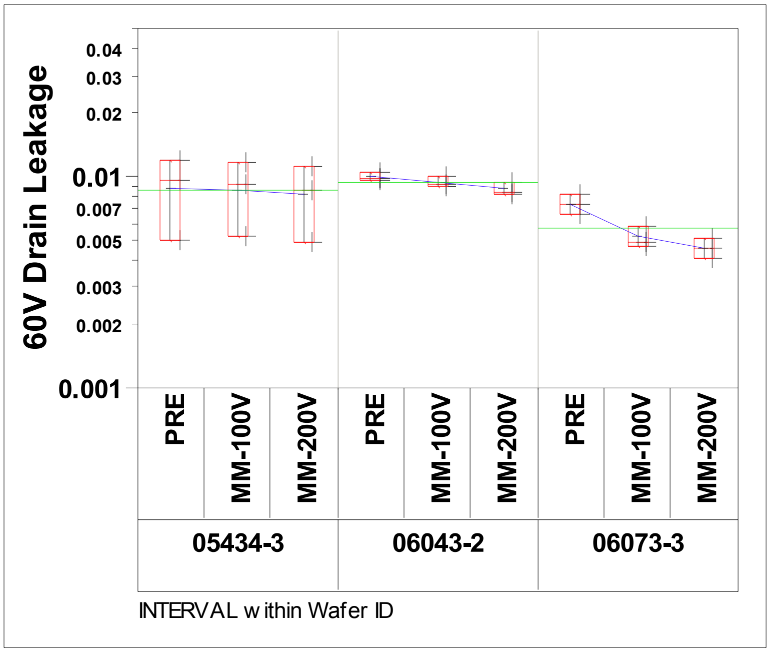

Figure 12: 60V Drain leakage shown on 3 wafers before stress and after stimulus with MM voltages of 100V and 200V. No failures or significant shifts in performance.

5.2.6 Thermal Impedance Results

Thermal impedance measurements were made using a QFI Infrascope II infrared thermal imaging microscope. The measurement was made with the heat sink temperature at 80°C and a thermocouple mounted below the package used to measure the case temperature. The bias condition was V_{DS}=28V and I_{DS}=975mA for each device, which is equal to the power dissipated under the RF operating point of P_{out}=6W and Efficiency = 18%. A total of 8 samples were measured from 3 wafers with all 8 devices at or below the datasheet spec of 1.95°C/W. Table 5 summaries the results on the 8 devices.

Table 5: Thermal Resistance measurements on NPT35050A:
Rth Specification = 1.95C/W.

DUT	T_{case} (°C)	$T_{junction}$ (°C)	R_{TH} (°C/W)	Pass/Fail
1	88.50	142.00	1.95	PASS
2	89.80	143.00	1.95	PASS
3	88.90	137.00	1.76	PASS
4	88.10	134.00	1.68	PASS
5	88.60	141.00	1.92	PASS
6	88.00	137.00	1.79	PASS
7	88.20	136.00	1.75	PASS
8	88.20	141.00	1.93	PASS
AVG	**88.54**	**138.88**	**1.84**	
STD DEV	**0.59**	**3.27**	**0.11**	

5.2.7 VSWR Robustness Testing

VSWR mismatch was presented to devices under operating conditions of V_{DS}=28V, I_{DQ}=750mA, P_{out}=38dBm and Frequency=3.5GHz with OFDM modulation applied. A total of 5 devices were stressed and characterization before and after stress shows no significant shift in performance as seen in Fig. 13.

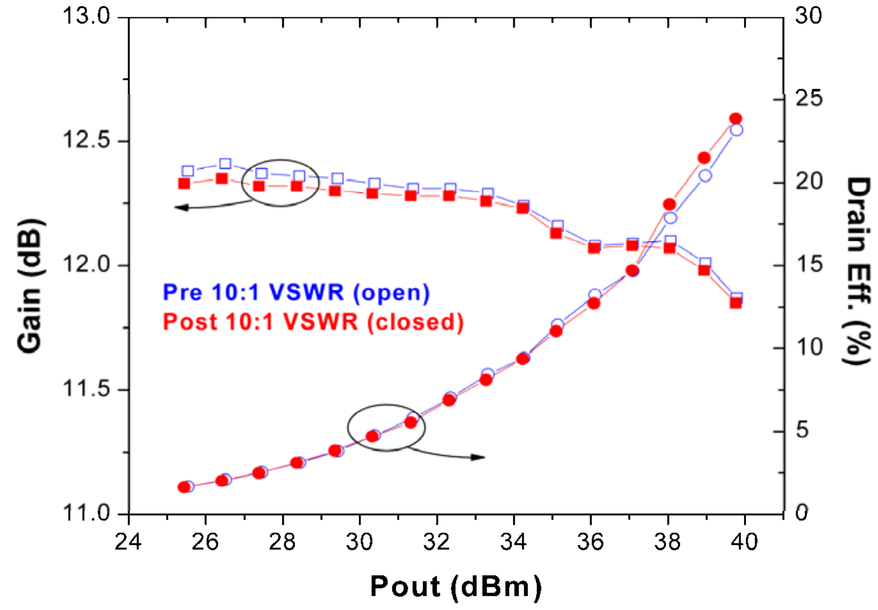

Figure 13: RF power sweep for typical device before and after stress with 10:1 VSWR mismatch.

5.2.8 Environmental Test Results

A number of environmental tests were performed including autoclave, temperature cycling, thermal shock, and bond strength. Autoclave, temperature cycling and thermal shock devices all passed with no degradation in performance. Bond pull results showed bond strength values 3x higher than the minimum requirement as seen in Fig. 14.

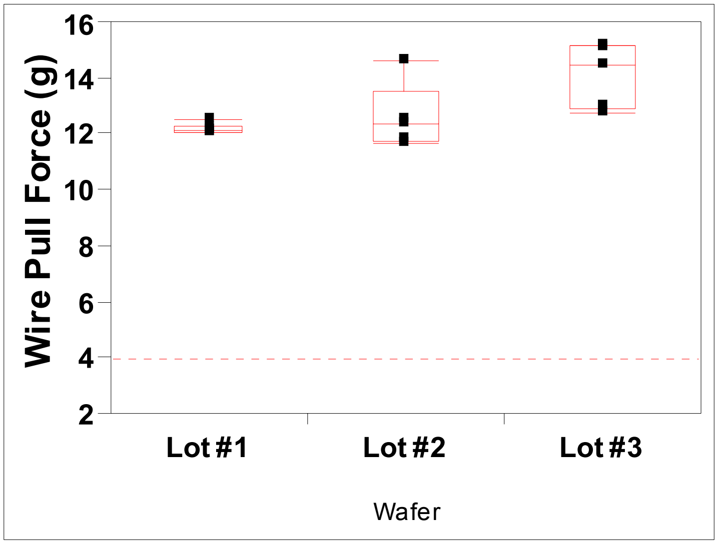

Figure 14: Bond Pull testing showing wire pull force 3X higher than minimum requirement.

5.2.9 Package Test Results

Additionally a number of package level tests were performed including mechanical shock, vibration, constant acceleration, solvent resistance, and salt atmosphere. No failures were seen on any tests.

6.0 Summary

This document outlined qualification of the NPT35050A device. Product qualification leveraged a consistent and reliable process platform, NRF1. Devices from the NRF1 process platform were built in ceramic packages and produced good CW and OFDM performance from 3.3 to 3.8GHz. This NPT35050A device was then put through an extensive battery of device and package reliability tests including DC-HTOL, 3-temperature DC, ESD, Autoclave, etc. The NPT35050A demonstrated reliable operation by passing all qualification tests and was officially qualified by the Nitronex TQRB on September 22, 2006.