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# NPT1007 Qualification Document

Revision 1.0

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## 1.0 Scope

This NPT1007 product qualification document describes the results of a comprehensive set of acceptance tests. The objective of this product qualification was to precipitate failures in an accelerated manner compared to normal use conditions. These tests are a composite of the suites of generally accepted tests that are required to qualify products for industrial and military applications. These tests are capable of stimulating and precipitating packaging and die-package interaction failures. A comprehensive set of tests have been performed to assess the package and die-package interaction reliability, and high temperature operating life (HTOL) testing has been used to confirm the die intrinsic reliability performance.

## 2.0 Reference Documents

The reliability plan is based on industry- and military-accepted standard documents and references therein, primarily:

JESD47F, "Stress-Driven Qualification of Integrated Circuits," (revision January 2007)  
MIL-STD-883G, "Test Method Standard – Microcircuits," (revision February 2006)

This document generally follows the structure of JESD47. Tests were added and sample sizes were adjusted to also cover the military applications.

## 3.0 Reliability Qualification

### 3.1 Objective

The objective of this reliability qualification is to ensure that the NPT1007 product made with the NRF1 die technology meets a generally accepted set of stress test driven qualification requirements for industrial and military applications.

### 3.2 Test Vehicle and Qualification family

The NPT1007 product consists of two separate NRF1 36 mm total gate periphery transistor die, fabricated using the qualified Nitronex NRF1 GaN-on-Si process technology flow NRF1\_04\_1.6.2 and mask set N05013. The 4 mil thick die is bonded using 420 °C AuSi die attach into the AC780B-4 ceramic lidded package, which has two gate and drain leads for the two 36 mm die, a CPC flange (Cu / Pressed Mo-Cu / Cu) and a 0.78 inch air cavity.

### 3.3 Qualification plan: stress tests and lot sampling

Table 1 lists the stress tests performed per the qualification plan. The mechanical reliability tests are to verify the packaging and die-packaging interaction reliability performance. HTOL was performed for 168 hours both to confirm device intrinsic reliability performance in the early life of the device, and to check for any die-package interactions. The wear-out intrinsic reliability performance of the NPT1007 is qualified by similarity to the NPT25100 and NPT35050A products. All of these products are based on the qualified Nitronex NRF1 process technology, which has demonstrated intrinsic reliability performance for 20 year

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product lifetime, through three-temperature DC life testing and RF high temperature operating life (RF-HTOL), as described in the Nitronex documents NGD-007, "NPT35050A Qualification Document," and NGD-025, "NPT25100B Qualification Document."

The devices sampled for test are composed of approximately equal numbers from:

- three wafers for HTOL and electrostatic discharge (ESD) sensitivity, sampled from the frozen process of record, to encompass process variability
- three packaging lots for temperature cycling and two packaging lots for mechanical shock, to encompass packaging and die-packaging interaction variability
- one packaging lot for moisture resistance (MR) and salt atmosphere (SA)

**Table 1. Required stress tests for product qualification.**

Stress	Abbr.	Reference	Stress Conditions	DUT Failure Criterion	Wafers	Units / wafer	Total units	Acceptance criterion
High temperature operating life	HTOL	JESD22-A108, JESD85	VDS=28V, TJ~200C, 168hr	Datasheet specification limits, and time dependent degradation equivalent to NPT25100	3	16	48	0 fail
ESD Human Body Model	ESD-HBM	JESD22-A114	See reference	10X change in leakage or catastrophic fail	3	3	9	Classification
ESD Charged Device Model	ESD-CDM	JESD22-C101	See reference	10X change in leakage or catastrophic fail	3	3	9	Classification
ESD Machine Model	ESD-MM	JESD-A115	See reference	10X change in leakage or catastrophic fail	3	3	9	Classification
Temperature cycling	TC	JESD22-A104	-65/+150C	Datasheet specification limits	3	25	75	500 cycles / 0 fail
Moisture resistance	MR	M-883-1004	See reference	Visual inspection per MIL spec only (mechanical samples)	1	15	15	0 fail
Salt atmosphere	SA	M-883-1009	Condition "A" - see reference	Visual inspection per MIL spec only (mechanical samples)	1	15	15	0 fail
<b>TOTAL</b>						<b>180</b>		

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### 3.4 Results

#### 3.4.1 Transistor Reliability - HTOL

The transistor intrinsic reliability of the NPT1007 has been verified through 168 hour HTOL at  $T_J = 200\text{ }^\circ\text{C}$ . The devices were biased using a common drain connection and separate gate bias circuits to achieve approximately equal current flowing through each of the two transistors in the package, so that each transistor experienced  $T_J = 200\text{ }^\circ\text{C}$ . Table 2 shows the wafer lot sampling. Of these devices, in the first 24 hours, 3/50 displayed anomalous behavior that is related to the test board fixtures and/or the test system. The remaining 47 devices were successfully biased and displayed drain current that decreased as a function of time, nearly saturating after 168 hours, as shown in Figure 1. (Note that the blip near 40 hours is a result of an electrical glitch associated with launching an unrelated test on the same test system at that time.) The 47/47 surviving devices demonstrate a least tolerable percent defect LTPD of 5. The in-situ time-dependent current behavior is comparable to the qualified Nitronex air-cavity products made with the NRF1 process technology.

Figure 2 shows that IDLK60 decreases by 25-50% after 168 hours of HTOL stress. Figure 3 shows that VP increases by 5-10% after HTOL. Figure 4 shows that RDON does not change significantly after HTOL. Figure 5 shows that IDMAX decreases by less than 2% for each lot after HTOL. The changes in these DC parameters are relatively minor and are well within product specifications. Intrinsic lifetime projections show that the percentage change of the median value of IDMAX versus accumulated time at HTOL conditions of  $T_J = 200\text{ }^\circ\text{C}$  is as good as or better than the demonstrated intrinsic reliability performance of the NRF1 platform technology that was qualified using the NPT35050A (6 mil die thickness), as well as the qualified product NPT25100 (4 mil die thickness). Figure 6, Figure 7, and Figure 9 show that there is negligible shift in G\_SS, P1dB, and DEFF\_SAT after HTOL. Figure 8 shows that P\_SAT decreases by approximately 0.09% after HTOL.

These results show that the intrinsic reliability performance of the NPT1007 is consistent with the demonstrated reliability performance of the platform NRF1 process technology, as described in the Nitronex document NGD-007, "NPT35050A Qualification Document".

• Table 2. Wafer lot sampling for HTOL.

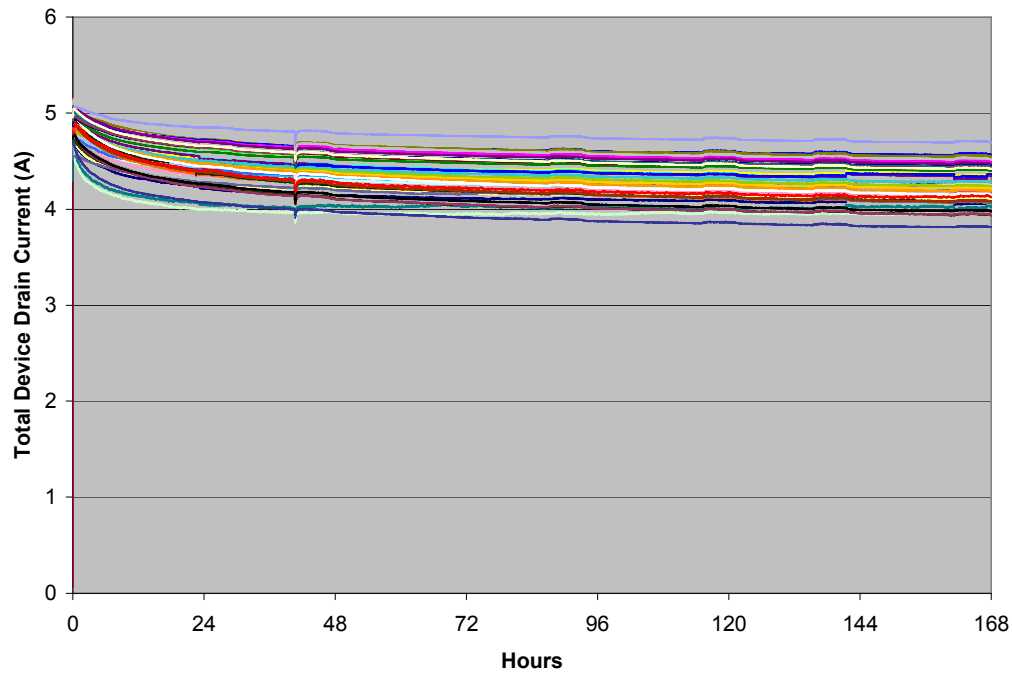
Wafer lot	Number of devices
08071-4	17
08280-2	16
08280-3	17

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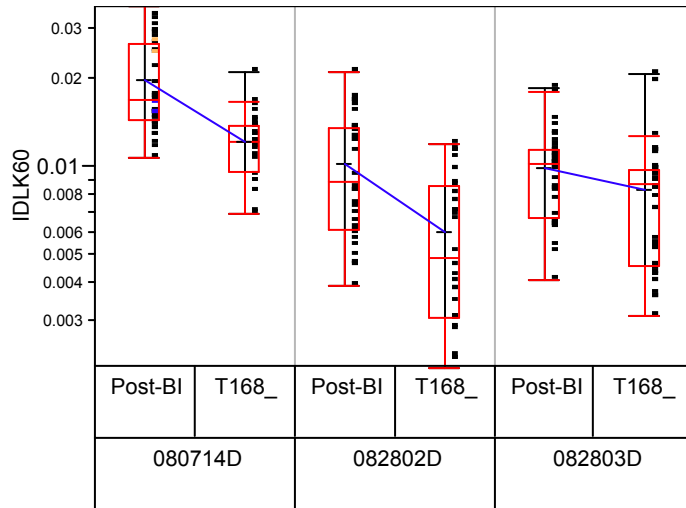
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• Figure 1. HTOL in-situ drain current versus time for 47 devices.

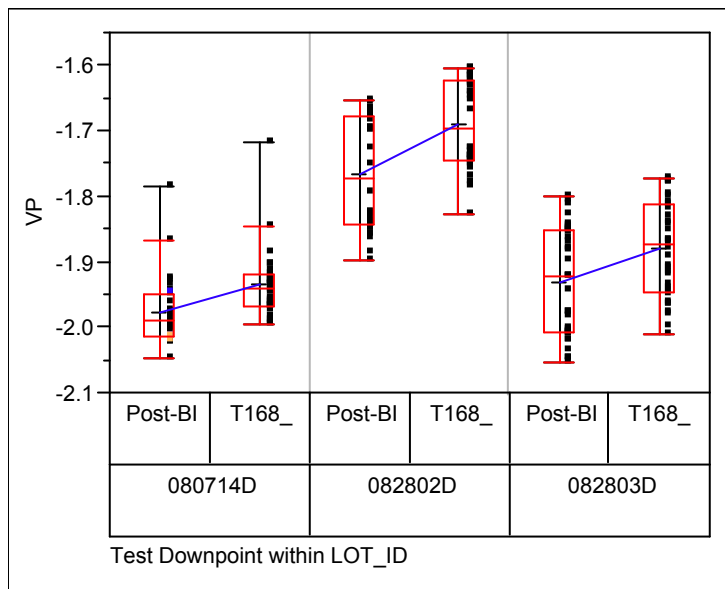
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Test Downpoint within LOT\_ID

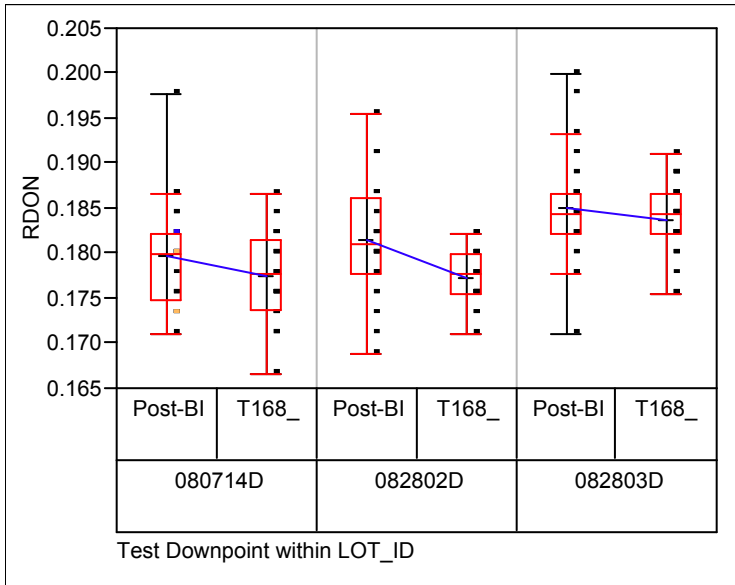
• **Figure 2. IDLK60 before and after HTOL.**



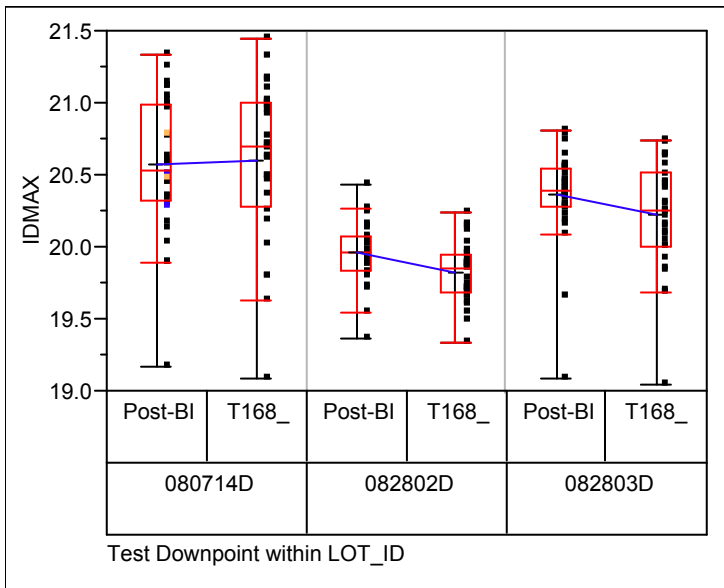
• **Figure 3. VP before and after HTOL.**

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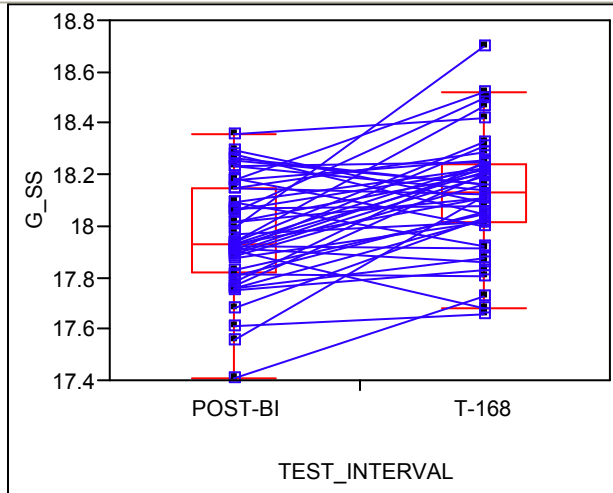
• Figure 4. RDON before and after HTOL.



• Figure 5. IDMAX before and after HTOL.

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**Oneway Analysis of G\_SS By TEST\_INTERVAL**

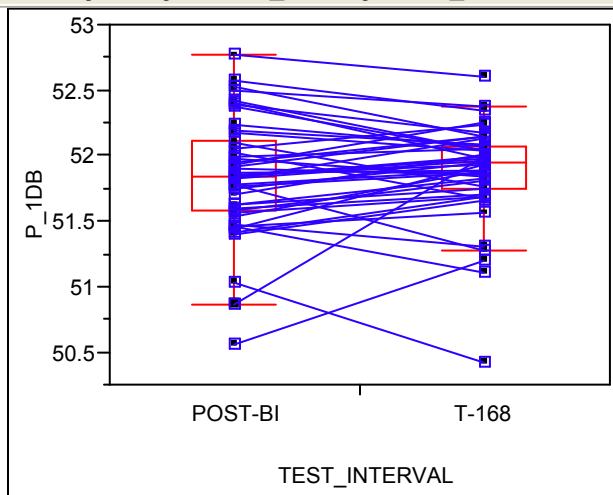


**Quantiles**

Level	Minimum	10%	25%	Median	75%	90%	Maximum
POST-BI	17.40822	17.73244	17.82724	17.9354	18.15148	18.26029	18.36257
T-168	17.66127	17.82491	18.01937	18.13506	18.24375	18.43792	18.70186

• Figure 6. Small signal gain before and after HTOL.

**Oneway Analysis of P\_1DB By TEST\_INTERVAL**



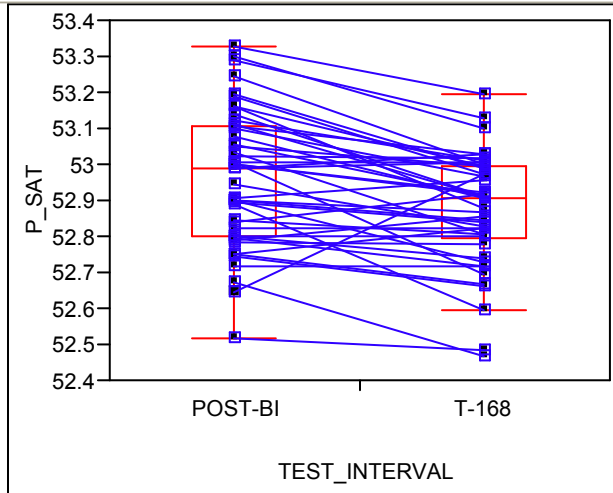
**Quantiles**

Level	Minimum	10%	25%	Median	75%	90%	Maximum
POST-BI	50.56946	51.41708	51.58575	51.84624	52.12675	52.45377	52.77658
T-168	50.41806	51.30589	51.74875	51.94786	52.07862	52.25295	52.61437

• Figure 7. Power at 1 dB compression before and after HTOL.

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**Oneway Analysis of P\_SAT By TEST\_INTERVAL**

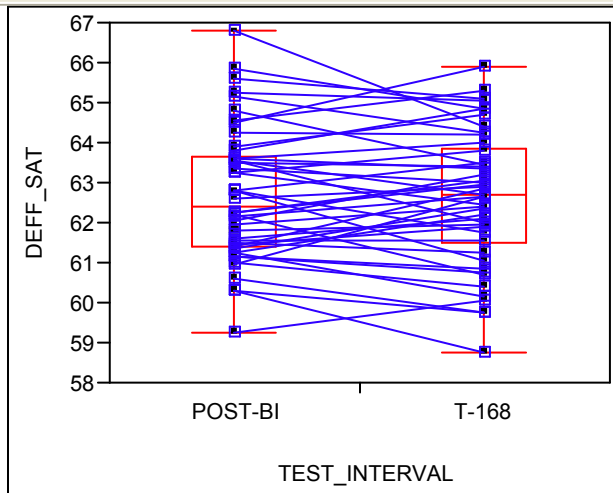


**Quantiles**

Level	Minimum	10%	25%	Median	75%	90%	Maximum
POST-BI	52.51974	52.73816	52.80367	52.99157	53.10813	53.21138	53.33012
T-168	52.46678	52.66661	52.7985	52.90908	52.99554	53.02836	53.19526

• Figure 8. Saturated power before and after HTOL.

**Oneway Analysis of DEFF\_SAT By TEST\_INTERVAL**



**Quantiles**

Level	Minimum	10%	25%	Median	75%	90%	Maximum
POST-BI	59.25337	60.86108	61.42059	62.44452	63.69403	65.20133	66.80448
T-168	58.75572	60.15093	61.51367	62.70232	63.88411	64.94865	65.94991

• Figure 9. Drain efficiency at saturation before and after HTOL.

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### 3.4.2 ESD

ESD sensitivity testing was performed on burned-in devices that met the target production DC and RF device specifications. ESD testing was performed by Integra Technologies.

#### 3.4.2.1 ESD-HBM

ESD Human Body Model (HBM) sensitivity testing was carried out in accordance with JEDEC specifications as follows:

- Perform curve traces on both transistor die separately for as-received devices.
- Apply a positive polarity (200 V) HBM pulse to each transistor die separately on each device.
- Perform curve traces - device failure is defined as either catastrophic or soft (IDLK > 10 mA) on either transistor die in the device. Passing devices continue to the next stress level.
- Apply a negative polarity (-200 V) HBM pulse to each transistor die separately on the same devices, i.e., do not use a fresh device for each voltage level.
- Perform curve traces.
- Repeat positive and negative polarity pulses at 500 V, 1000 V, 2000 V, and 4000 V and curve traces on the same devices until failure is observed on either transistor die in the device.

The results in Table 3 show that all of the devices tested survived pulses up to a level of +/-1000 V. 2/9 devices failed after pulses of -2000 V, and 7/9 devices failed after pulses of -4000 V. The failures all occurred after negative polarity pulses, and all on the Gate1 pin. The results demonstrate an ESD-HBM rating of 1C for the NPT1007.

- **Table 3. ESD-HBM results by lot. Pre-fail = device met specifications after that cumulative ESD pulse level; post-fail = the device failed after that cumulative ESD pulse level. The results demonstrate an ESD-HBM rating of 1C for the NPT1007.**

Lot number	Device number	Pre-fail (V)	Post-fail (V)
082803D	H1	2000	-2000
082803D	H2	4000	-4000
082803D	H3	4000	-4000
080493D	H4	4000	-4000
080493D	H5	4000	-4000
080493D	H6	4000	-4000
080714D	H8	4000	-4000
080714D	H7	4000	-4000
080714D	H9	2000	-2000

#### 3.4.2.2 ESD-CDM

ESD Charged Device Model (CDM) sensitivity testing was carried out in accordance with JEDEC specifications as follows:

- Perform curve traces on both transistor die separately for as-received devices.
- Apply three positive polarity (100 V) CDM pulses to each transistor die separately on each device.
- Perform curve traces - device failure is defined as either catastrophic or soft (IDLK > 10 mA) on either transistor die in the device. Passing devices continue to the next stress level.
- Apply three negative polarity (-100 V) CDM pulses to each transistor die separately on the same devices, i.e., do not use a fresh device for each voltage level.

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- Perform curve traces.
- Repeat positive and negative polarity pulses at 200 V, 500 V, and 1000 V and curve traces on the same devices until failure is observed on either transistor die in the device.

The results show that all 9/9 of the devices tested within specification after through all of the stress levels completed, through 1000 V CDM stress with both polarities. No failures were observed. The results demonstrate an ESD-CDM rating of “IV” for the NPT1007.

### 3.4.2.3 ESD-MM

ESD Machine Model (MM) sensitivity testing was carried out in accordance with JEDEC specifications as follows:

- Perform curve traces on both transistor die separately for as-received devices.
- Apply a positive polarity (100 V) MM pulse to each transistor die separately on each device.
- Perform curve traces - device failure is defined as either catastrophic or soft (IDLK > 10 mA) on either transistor die in the device. Passing devices continue to the next stress level.
- Apply a negative polarity (-100 V) MM pulse to each transistor die separately on the same devices, i.e., do not use a fresh device for each voltage level.
- Perform curve traces.
- Repeat positive and negative polarity pulses at 200 V and 400 V and curve traces on the same devices until failure is observed on either transistor die in the device.

The results in Table 4 show that all of the devices tested survived pulses up to a level of 100 V. 4/8 devices failed after pulses of 200 V, while the other devices failed after higher voltage pulses or not at all. The failures all occurred on the Gate1 pin. The results demonstrate an ESD-MM rating of “A” for the NPT1007.

- **Table 4. ESD-MM results by lot. Pre-fail = device met specifications after that cumulative ESD pulse level; post-fail = the device failed after that cumulative ESD pulse level. One device was excluded because the as-received device displayed out-of-specification curve trace results. The results demonstrate an ESD-MM rating of “A” for the NPT1007.**

Lot number	Device number	Pre-fail (V)	Post-fail (V)
082803D	M1	400	-400
082803D	M2	400	-400
082803D	M3	-100	200
080493D	M4	-400	n/a
080493D	M6	-100	200
080714D	M7	-200	400
080714D	M8	-200	200
080714D	M9	-200	200

## 3.4.3 Packaging and Die-Package Reliability

### 3.4.3.1 Temperature cycling

The device temperature cycling reliability has been demonstrated by showing that 75/75 devices successfully survived 500 cycles from -65 °C to +150 °C, with no significant change in electrical performance. Scanning acoustic microscopy on a sampling of those devices showed no significant die attach void growth or die cracking after temperature cycling.

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### 3.4.3.2 Mechanical shock + vibration + constant acceleration

The device mechanical reliability has been demonstrated by test results showing that 20/20 devices successfully survived the mechanical shock + vibration + constant acceleration suite of stressing, with no significant change in electrical performance.

### 3.4.3.3 Moisture resistance

The package moisture resistance has been demonstrated by showing that 15/15 packages meet the MIL standard visual inspection acceptance criteria after moisture stress.

### 3.4.3.4 Salt atmosphere

The package salt atmosphere resistance has been demonstrated by showing that 15/15 packages meet the MIL standard visual inspection acceptance criteria after salt atmosphere stress.

## 4.0 Summary

In summary, the NPT1007 meets reliability performance requirements for HTOL, thermal cycling, mechanical shock, vibration, constant acceleration, moisture resistance, and salt atmosphere, per the qualification plan. The ESD reliability performance has been characterized using the HBM, CDM, and MM methodologies.

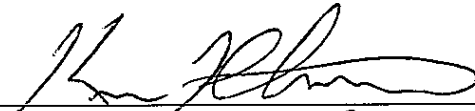
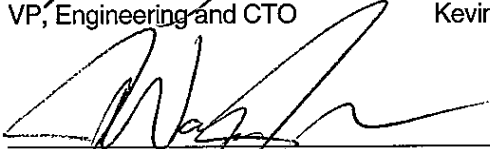
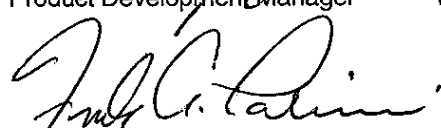
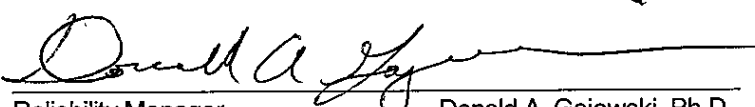
Stress	Abbr.	Result
High temperature operating life	HTOL	0 fail; intrinsic lifetime projection similar to NRF1 process qualification
ESD Human Body Model	ESD-HBM	>1000V (Class 1C)
ESD Charged Device Model	ESD-CDM	>1000V (Class IV)
ESD Machine Model	ESD-MM	>100V (Class A)
Temperature cycling	TC	0 fail; minimal change in performance
Moisture resistance	MR	0 fail
Salt atmosphere	SA	0 fail

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**5.0 Approval List**

	<u>1/21/09</u>
VP, Engineering and CTO      Kevin Linthicum, Ph.D.	Date
	<u>1/25/09</u>
Product Development Manager      Wayne Johnson, Ph.D.	Date
	<u>1-27-09</u>
Quality Manager      Frank A. Palmieri	Date
	<u>1/19/09</u>
Reliability Manager      Donald A. Gajewski, Ph.D.	Date

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