# GaN Essentials™

# AN-009: Bias Sequencing and Temperature Compensation for GaN HEMTs

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## 2. Abstract

This application note will discuss fundamental usage methodologies to design with GaN HEMT devices. Specifically, this discussion will center on proper biasing techniques as well as temperature compensation surrounding GaN HEMT technology. A bias sequencing circuit and a temperature compensation circuit will be presented.

## 3. Bias Sequencing and Temperature Compensation

The biasing of high power RF devices, especially GaN devices, requires special attention. The concerns are mainly for preventing instabilities or oscillations, maintaining large drain current with a small voltage drop, and bias decoupling circuits to reduce interference with the RF matching circuit as well as limiting its influence on the linearity of the device. Also, properly maintaining the device current over temperature improves the performance in multiple operating environments. This application note will address the issues associated with biasing, bias sequencing and temperature compensation of a Nitronex GaN HEMT.

GaN HEMTs are depletion mode devices which require a negative voltage applied to the gate. Supplying a negative voltage on a lab bench is easily accomplished by either using a supply with negative voltage generation capability or by switching the leads between the ground node and the positive voltage node. In a typical application circuit the negative voltage comes from a regulator or a negative voltage generator.

### 3.1. Bias Sequencing

For GaN HEMT devices, the first and most important issue is the biasing sequence. The goal while biasing the device is to stay away from areas which are sensitive to the potential instability of the device, for instance, the area where $V_{DS}$ is low and $I_{DS}$ is high. Assuming that the device is properly connected to a regulated power supply and that the drain and the gate are sufficiently DC decoupled and connected to 50 Ohm terminations the recommended bias sequence is as follows:

- Set $V_{GS}$ = 0V (gate), and $V_{DS}$ = 0V (drain).
- Decrease $V_{GS}$ to the Pinch-off voltage ($V_P$), typically -1.8 to -2.2V for Nitronex's GaN devices.
- Increase $V_{DS}$ up to the nominal voltage.
- Increase $V_{GS}$ until the required quiescent current is reached.
- Apply the RF power.

Similarly, the recommended turn-off sequence is as follows:

- Turn off the RF power.
- Decrease $V_{GS}$ down to $V_P$.
- Decrease $V_{DS}$ down to 0V.
- Set $V_{GS}$ to 0V

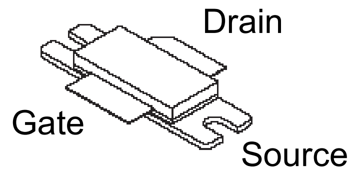


**Figure 1. Packaged device lead identification for Nitronex's GaN HEMT device.**

## 3.2. Gate Power Supply Needs

One needs to pay attention to how to deal with a positive gate current which will arise when the device is driven hard. Many commercial power supplies are not able to source and sink DC current through the same connector. One way to overcome this limitation is to use a resistor connected across the power supply terminals, this resistor will enable the power supply to always provide a negative current while allowing the device to source or sink current. The maximum value for this resistor is determined by the gate voltage and the amount of gate current required by the device. This can be calculated by the following:

$$R_{MAX} = \frac{-V_{GSMAX}}{I_{GSMAX}}$$

A 50W Nitronex device has nominal $V_{GSQ}$ between -1.2V and -1.6V, and an $I_{GSMAX}$ = 20mA.

Moreover, the resistor's power rating also needs to be considered when selecting a gate resistor. For instance, with $V_{GSQ, MIN}$= -2 V, and 20 mA current a 100 Ohm gate resistor dissipates 0.04 W; therefore at 0.10 W resistor can be safely used.

**Table 1. Quiescent and saturated gate current vs device periphery**

| Nitronex Device | Device Periphery (mm of Gate Width) | $I_{GS,MAX}$(mA) (RECOMMENDED OPERATING) | $I_{GS,MAX}$(mA) (ABSOLUTE MAXIMUM) |
|---|---|---|---|
| NPTB00004 | 2 | 2 | 10 |
| NPTB00025 | 8 | 8 | 40 |
| NPTB00050 | 16 | 16 | 80 |
| NPT25100 | 36 | 36 | 180 |

When using a resistor at the gate feed line to suppress oscillation, its value should be properly selected to keep $I_{DS}$ constant versus $RF_{IN}$. The reason for this is $I_{GS}$ can change from negative to positive and cause $V_{GS}$ variation. To limit $V_{GS}$ variation to a small level the maximum value of the gate resistor should be limited to:

$$R_G = \frac{-V_{GSMAX}}{I_{GS,MAX}}$$

Lumped capacitors can be used for DC blocking for applications at S band and below to isolate the source and load from $V_{GS}$ and $V_{DS}$. DC blocking capacitors are selected to have the series resonant frequencies in the bandwidth of interest to achieve low impedance as much as possible for these capacitors. They are also selected to have high Q's to have minimum insertion loss. The breakdown voltage of these DC blocking capacitors needs to cover the maximum voltage (DC + RF) they will be subjected to.

To accommodate the high drain current, and to achieve the lowest voltage drop and lowest cost, a microstrip line feed is recommended. A quarter wave line shorted at one end will provide an RF open at the other end to prevent RF leakage.

## 3.3. Temperature Compensation

After making sure that the device is turned on and operational, proper care must be taken to adequately bias the device for consistent performance versus temperature. The quiescent current of a GaN HEMT device is primarily a function of temperature and $V_{GS}$. Maintaining consistent performance can be accomplished by designing a bias circuit around the device so as to maintain a constant $I_{DSQ}$. As the graph shows below, $V_{GS}$ changes proportionally to IDS and temperature. For instance, a typical 90W GaN HEMT device needs $V_{GS}$ = -1.58 at a -40C base plate, and $V_{GS}$ = -1.46V at a +85 C baseplate to maintain $I_{DSQ}$ = 700 mA.

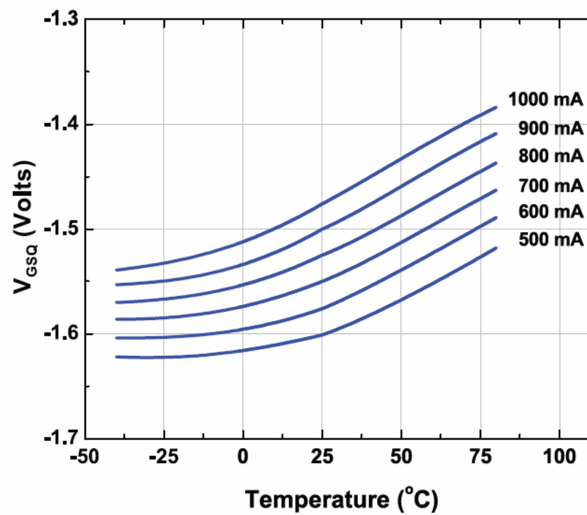


**Figure 2. Quiescent Gate Voltage Required to Reach $I_{DQ}$ as a function of Case Temperature**

Given the above curves, a circuit needs to be developed to follow this shape as closely as possible to maintain constant $I_{DSQ}$. Such a circuit has been developed to take into account the need for constant $I_{DSQ}$ as well as the items mentioned above with respect to bias sequencing, and the gate power supply needs. One such implementation for bias sequencing and gate bias control is shown below. This circuit supplies a temperature compensated voltage to the gate. This circuit also includes the proper sequencing of gate and drain power supplies to operate the part in a safe operating region to keep from damaging the device.

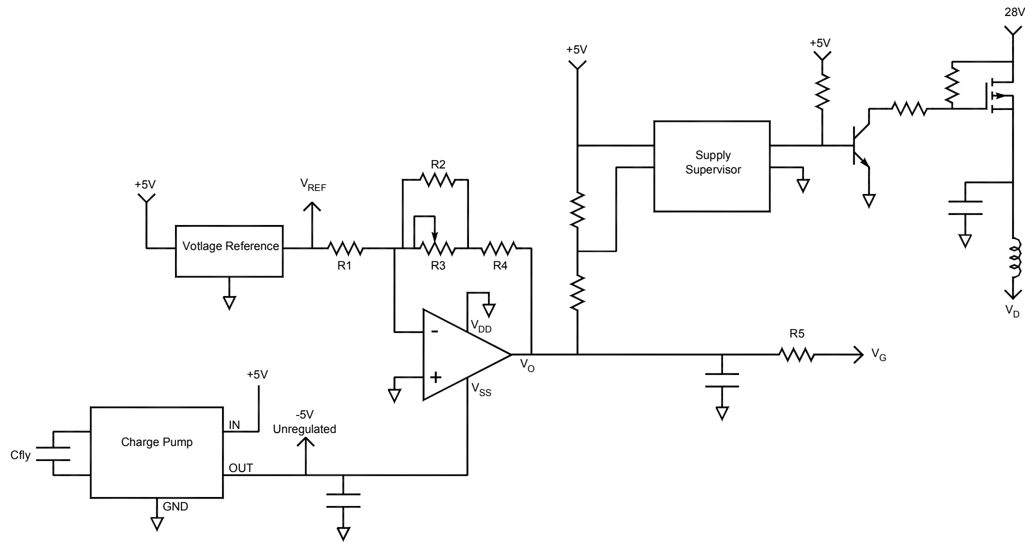


**Figure 3. Recommended Bias Circuit for Temperature Compensation and Bias Sequencing**

**Note: R3 is a thermistor.**

The above circuit uses an N-channel MOSFET as a high-side switch to deliver VDS to the GaN HEMT. It is important to properly size this FET relative to the size of the HEMT being biased, in terms of $R_{DSON}$, $R_{TH}$, and $V_{DSMAX}$. In general, smaller gate periphery HEMTs can be switched with smaller- and less expensive – MOSFETs. Specifically, $R_{DSON}$ is selected to keep the voltage drop across the switch for a given maximum $I_{DS}$ below a user-selected tolerance value:

$$R_{DSON} < \frac{V_{drop}}{I_{DS\max}}$$

Of course, $V_{DSMAX}$ must exceed the maximum switched drain supply voltage by a user-selected margin. And finally the MOSFET should have an $R_{TH}$ which ensures that its maximum junction temperature is not exceeded even when the HEMT is drawing its maximum current (and the MOSFET is experiencing maximum power dissipation). As examples, a small 2mm HEMT may be safely switched with a small, inexpensive MOSFET with $R_{DSON}$ as high as 500 milliohms in a SOT223-4 package. Larger 8mm and 16mm devices should use MOSFETs which keep $R_{DSON}$ below about 150 milliohms and be housed in a DPAK or similar package with sufficient heat sinking. Even larger 36mm devices require switches with sub-80 milliohm $R_{DSON}$ and packaging that will dissipate several watts.

The above circuit utilizes a charge pump to supply the necessary negative voltage rail to the operational amplifier (assuming that a suitable system negative voltage is not already available). The op amp must be capable of supplying the maximum negative and positive gate current for the HEMT being biased, and the charge pump must be capable of supplying the maximum negative current needed for that circuit. The positive terminal of the op-amp is grounded while the other is fed from a voltage reference supplying 1.25V to the feedback circuit around the op-amp. In the feedback circuit there is a thermister which changes resistance proportionally to the temperature. As the thermister changes, the transfer function and therefore the output voltage of the op-amp circuit is modified which supplies the gate voltage to properly bias the

device. The gate voltage is monitored by a supply supervisor circuit that once it senses the gate voltage outputs a voltage to a pair of pass transistors. These pass transistors control the application of the drain voltage. Therefore the above circuit accomplishes the necessary temperature compensation of the gate voltage to maintain a constant $I_{DSQ}$, but also the bias sequencing discussed in the beginning of this document.

The transfer function of the operational amplifier is given by the following equations:

$$V1 = \left(\frac{-VREF}{R1}\right)\left(\frac{R2R3}{R2+R3}\right)$$

$$VO = \left(\frac{-VREF}{R1}\right)\left(\frac{R2R3}{R2+R3}\right)\left(\frac{R2R3+R3R4+R2R4}{R2R3}\right)$$

$$VG = \left(1+\frac{R5}{R4}\right)VO - \left(\frac{R5}{R4}\right)V1$$

Using the spreadsheet located on the GaN Essentials webpage, the values of resistors in the temperature compensation circuit can be determined for particular $V_{GSQ}$ at 25°C case temperature. (Click the link located at http://www.nitronex.com/ganessentials.html to open the file.)

**Table 2. Resistor values for fixed $V_{GSQ}$ at 25° C case temperature**

| $V_{GSQ}$ (V) at 25C | R1(Ω) | R2(Ω) | R4(Ω) | R5(Ω) |
|---|---|---|---|---|
| -1.6 | 10k | 3k | 10k | 10 |
| -2.0 | 10k | 3k | 13.2k | 10 |
| -2.5 | 10k | 3k | 17.2k | 10 |
| -3.0 | 10k | 3k | 21.1k | 10 |

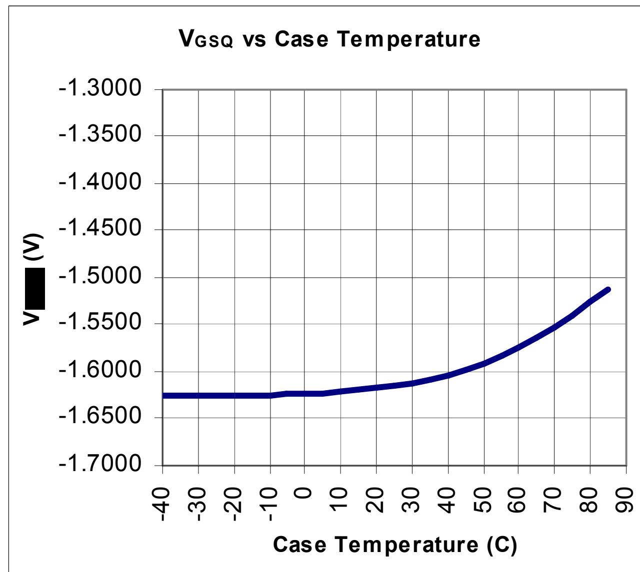


**Figure 4. Modeled $V_{GSQ}$ vs Case Temperature for Temperature Compensation Bias Circuit**

The graph above shows the output from the spreadsheet of how the above circuit would behave versus temperature. As Table 2 shows, the value of R4 was modified to adjust the gate source voltage for Class-AB operation around -1.6 V through Class-C and deep Class-C operation from -2 to -3 V.

## 3.4. Conclusion

In conclusion, this application note describes the proper sequencing necessary to properly turn on a GaN HEMT device. Furthermore, this application note described some of the necessary requirements for the gate bias power supply. Lastly, this application note demonstrates an active bias circuit that compensates for the $I_{DSQ}$ change versus temperature to maintain a constant $I_{DSQ}$ and the proper bias sequencing.